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THESIS

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Master of Science Degree

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REALIZATION OF A DIGITAL COMPUTER LABORATORY CAPABILITY

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Preface

This thesis is a result of an analysis of contemporary commercial equipment that can be used to realize a digital computer laboratory capability and a result of an attempt to compile experiments that can demonstrate computer theory on the selected equipment. There are two basic approaches that can be taken to solve this problem. The experiments can be written, and then equipment can be selected to demonstrate the experiments. Conversely, it is possible to select the equipment and then to write experiments that can be performed on the equipment. The latter method was chosen with the stipulation that the equipment had to meet certain broad requirements. These requirements were established, the equipment was selected that satisfied these requirements, and finally experiments were written that could be easily realized on the equipment.

This thesis is written to be read by people that have a fundamental knowledge of computer logic, electronic circuits, and Boolean algebra (including Karnaugh maps). The experiments described in this thesis can only be performed on equipment not yet prossessed by the Institute.

I would like to express my appreciation to Captain Mathew Kabrisky for his guidance throughout the period that I was involved in this project. Also, I would like to acknowledge the assistance of the Engineered Electronics Company and their local representative, the R.M. Odell Company, who loaned us one of their Digital Bread Boards.

George W. McKemie.

Abstract

There is a definite requirement within the Institute of Technology for digital computer laboratory capability. There are several commercial companies who market digital equipment that could be used in the laboratory. The best device to satisfy the Institute's requirements appears to be Engineered Electronic Company's Digital Bread Board. This unit is a solid state trainer used for bread boarding electronic systems. Experiments are written fully demonstrating the essentials of basic computer logic. The thesis ends with the recommendation to obtain the capability described within.

Contents

Contents

REALIZATION OF A
DIGITAL COMPUTER LABORATORY CAPABILITY

I. Introduction

Background

The Electrical Engineering Department of the Institute has established a requirement for the development of a digital computer laboratory capability to be used in conjunction with Electrical Engineering Course EE-309, Digital Computer Circuitry. Theoretical realization of this capability is the purpose of this thesis. Primary purpose of this thesis is the development of laboratory experiments that can be used in this course. Secondary consideration will be given to selection of the hardware to perform this task.

Purpose

This thesis is intended to develop a theoretical capability for a digital computer laboratory. There are two main areas in which work must be accomplished. First and most important, laboratory experiments must be written. The experiments must demonstrate the theory of the present digital computer circuits course. Second, a survey must be made of the equipment that is capable of performing these experiments, and a recommendation made as to what is the most advantageous method to be used in the proposed laboratory.

Scope

This thesis will not attempt to develop any of the theory behind digital computer circuitry or logic. The reader is presumed to have a broad knowledge in this field. The experiments themselves are written with the understanding that they will be used in conjunction with a theory classroom course; therefore, the experiments do not explain in great detail the theory behind the principles that they demonstrate.

The survey of existing equipment to perform the laboratory functions is based upon all the known commercial equipment at the time of compiling the data. Time precluded a complete investigation of the possibility of locally designing and manufacturing the required equipment within the capabilities of the Institute, but it seems apparent that no great advantage could be achieved by this method.

Engineered Electronics Company was kind enough to make available the use of one of their Digital Bread Boards for evaluation. Extensive work was done on this machine to understand its full capabilities. There will be no lengthy discussion of this work except when it is reflected in the development of one of the experiments.

Plan of Development

The remainder of the body of this thesis is divided into four more chapters. Chapter II is concerned with a survey of existing

laboratory equipment. Criteria are established which the equipment must satisfy. A brief discription of the various equipment is presented. A comparison of the equipment is made prior to establishing the Engineered Electronics Company's Digital Bread Board as the device best suited to the Institute's requirements. The chapter concludes with a short description of the Digital Bread Board.

Chapter III discusses the experiments. A list of the experiments is given, and the assumptions listed that was used in writing the experiments. The experiments are discussed and pertinent comments are made.

Chapter IV discusses some of the cost considerations. A final cost estimate to achieve minimum laboratory is made. It is estimated that it would require approximately $8878.00 to achieve minimum capability. For a somewhat lesser cost, some equipment could be purchased and used fairly efficiently.

Chapter V is used to make recommendations. The laboratory is feasible at a not unreasonable sum. This thesis recommends immediate action to achieve this capability. The chapter concludes with some recommendations on future study in this area.

The laboratory experiments themselves are included in Appendix A. The present Electrical Engineering Department laboratory format is preserved at the risk of deviating slightly from thesis format. The figures in the experiment are considered as part of the experiment itself and are not considered germane to the thesis. For

this reason they are not listed in a list of figures. These experiments represent the main expenditure of work.

Appendix B gives a breakdown on the total cost of the Digital Bread Board.

Included as Appendix C to the thesis is the EECo Catalog. This catalog gives a complete breakdown on the electronic design of all modules used in the Bread Board.

II. Survey of Existing Digital Laboratory Equipment

Comparison and selection of the equipment that is to be used in realization of the laboratory must be based on several factors. The first criteria is the capability of the equipment to perform the experiments necessary to demonstrate the important theory in the course. In addition the equipment should have the capability of demonstrating the logic in such a manner that the logic theory is not hidden by the electronic features of the equipment. The final factor is the cost consideration.

Equipment

This section will be devoted to description of the various types of digital equipment that were considered.

Univac Digital Trainer. This trainer is a general purpose computer designed for use in a maintenance or programming type course. It is a complete computer having a wide variety of arithmetic commands and a 512 word core memory. It includes some input/output equipment. (Ref 13:2) Estimated cost of this machine is well in excess of $10,000.

Jackson Instruments Pro-Log Model LS-MK-1. The Pro-Log is a large trainer that demonstrates the logic functions by use of mechanical relays. These relays can be used in various types of gating circuits to synthesize logic functions. The large unit has receptacles for 144 plug in units. In addition there are smaller

portable units that can be used in the classroom. A small version of this trainer was loaned to the Institute of Technology for evaluation. Cost of this device is $7000.

DEC Classroom Modules. Digital Electronic Equipment markets a series of laboratory modules capable of 500 kilocycles operation (Ref 4:2). This modules, referred to as DEC 3000 Series, contain complete logic functions within themselves. These modules can be combined together in such a manner that they can perform computer functions. External power connections must be supplied to the system. Modules of similar nature are marketed by such companies as Control Logic Corporation and Engineered Electronics Company. The operating frequency differs, but the same principles apply.

Classroom Trainers. Two companies, Control Logic Inc. and Engineered Electronics Company, produce classroom trainers. The Control Logic devices is designated as the PE 1 Programmable Digital Training Systems (Ref 8:1-6); the Engineered Electronics trainer is called a Digital Bread Board (Ref 5:66). In operation both of these systems are similar. Both contain integral power supplies and have the capability to have input/output equipment attached to them. Both systems operate at a relatively low clockrate, which is not a handicap for this type of application. The main difference of these two systems is the manner in which they are logically constructed. The Digital Bread Board consists of separate logic

units. In general, each device (flip flop, delay, gate, etc.) is contained in a separate unit, capable of being purchased as that unit. This type of construction is not duplicated in the PE 1 systems. In the PE 1, the units are arranged in panels. In one panel, the PF1-Pulse Forming Circuits Panel, there are some 16 individual logic devices. In order to buy one of the logic circuits, it is necessary to buy the entire panel (Ref 10:1-6). The Storage Register Flip Flop Panel of the PE1 systems consists of eight storage flip flops, one power amplifier, one pulse shaper, and one register reset toggle switch (Ref 10:6). The panel costs $280 (Ref 14). Assuming equal cost of each of the ten electronic devices on the panel, the cost of each flip flop is $28. A flip flop, T-101B, for the Digital Bread Board bought in quantities of 25 or more costs $27.10 (Ref 12:1). While this is just one example of cost comparison, it is possible to note that there is not a great deal of difference in the costs of the two systems.

Selection of a Digital Trainer

It is possible to eliminate the Univac Digital Trainer at once. This system does not fulfill the first requirement of having the capability to perform the experiments. It is designed to be used by programmers and maintenance personnel; hence, it is not reasonable to expect it to fulfill the requirements for a logic circuits course.

The Jackson Instruments Pro-Log fails to completely meet the requirement to perform its function in such a manner that the logic

is not obscured by the electrical complexity of the system. Its flexibility is somewhat limited and it would be difficult to expand the system to any extent using relay logic. Adaptation of the equipment into a course that emphasized electronic circuitry as well as logic would be impossible. The high cost, $7000, makes these shortcomings extremely unattractive.

The modular approach fulfills the first two conditions stated at the beginning of the chapter. They are capable of performing any desired experiment in such a manner that the logic of the system is not hidden. The cost of the 500 kilocycle DEC 3201 flip flop is $63 (Ref 4). This cost, more than twice as much as the cost of the flip flops in the classroom trainers, eliminates this modular construction. The other companies that make the modules (Control Logic and Engineered Electronic) also make the classroom trainers. It is found that their approach to solution of the classroom problem is through the use of these trainers. Their modules are not competitive with their trainers for classroom application.

By a process of elimination, the choice is narrowed to one of two types of classroom trainers. This fact is not surprising as a system designed for one particular use will generally compete more favorably for that one use, than will a system that is primarily designed for something else. The two systems have comparable unit cost and capability. There is one major difference. As previously

noted, the Digital Bread Board can be bought in individual logic units while the Pe-l systems must be bought in panels. This would tend to make purchase of the Bread Board more flexible. It is this flexibility that makes the Bread Board a more attractive choice as the equipment to be used in the digital computer laboratory. All of the experiments have been designed with the idea that they will be performed on the Engineered Electronics Company's Digital Bread Board.

The Digital Bread Board

The Digital Bread Board, manufactured by Engineered Electronics Company of Santa Ana, California, can be either rack mounted or suitcase mounted. Fig. 1 and 2 show the suitcase mounted configuration. The board shown can accommodate bread board systems of up to 24 modules. Another version of the same trainer can increase this capacity to 32 modules.

The modules are incapsulated into cans containing the entire logic device circuitry. Each module is inserted into the receptacles in such a way as to preclude inadvertent application of the wrong voltage to the wrong pin. Care must be taken to insure that the modules are inserted straight in order that the pins are not bent.

The individual modules are connected together by external connections. The signal path is from one module to the next via the external connections. Each module can be monitored by connecting its output to an indicator light located on the bread board. All connections are made external to the Bread Board. There is never

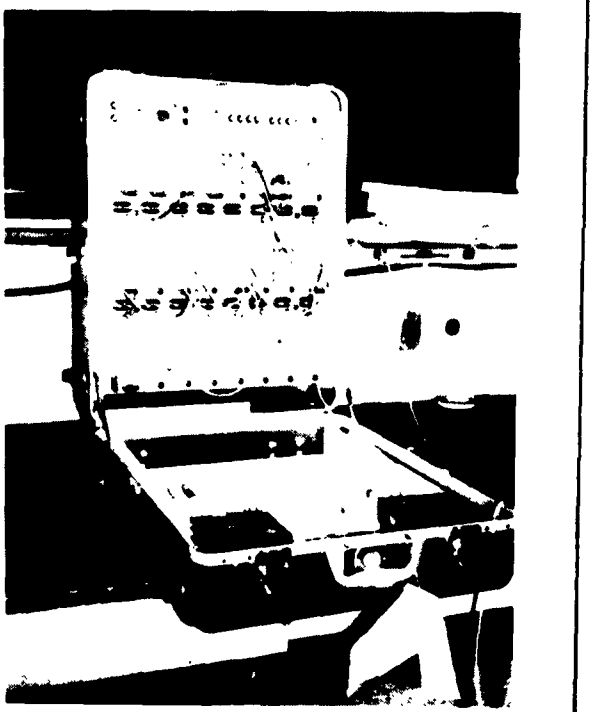


Fig. 1

EECo Digital Bread Board

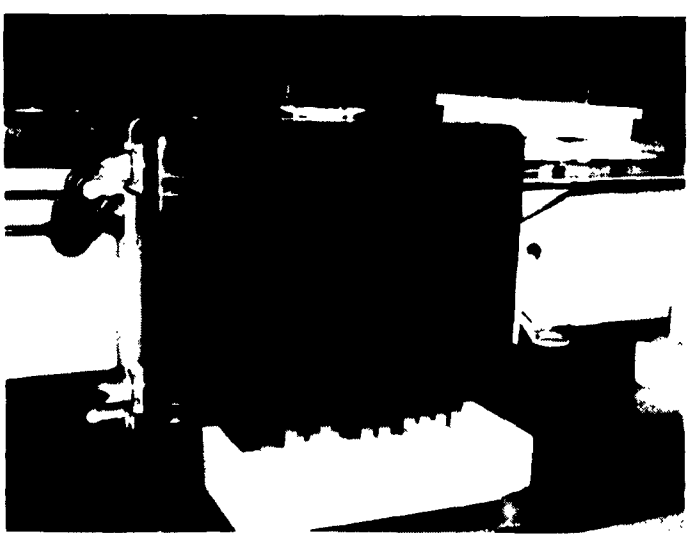


Fig. 2

EECo Digital Bread Board

any requirement for the student to open one of the modules.

Table I gives the electrical and physical specifications of the trainer. Another convenience is that the suitcase is mounted on casters to aid in moving it from one place to another. The available voltages can be paralleled to another rack that does not contain its own internal power supply.

Table I
Specifications
of
Digital Bread Board

Input Power	
Voltage	115 ± 10%
Frequency	50-400 cps
Power	30 watts
Capacity	24 modules
Voltages Available	12VDC, 6VDC, -3VDC, -11VDC
Size	24" x20" x9"
Weight	40 lbs. (Total)

(Ref 5:69)

Engineered Electronics Company provides a warrantry to their equipment to the extent that a module failing in normal service due to defective parts, workmanship, or packaging will be replaced without charge providing parts are still available. Modules defective for some other reason can be repaired at cost (Ref 12:9).

The equipment appears to be well engineered. The modules have good solder joints; the entire workmanship is neat and professional. Many of the modules have internal emitter followers, providing the equipment with good output characteristics. It is possible to drive as many as six output from one "And" gate without noticing any

degradation of the signal level. This capability is not included in the flip flops. At the lower frequencies of the trainer, synchronization does seem to be a problem. The rise time of the modules is approximately 0.5 microseconds. Little or no delay was observed through six cascaded modules. Level restoration does not appear to be a problem for normal laboratory experiments. Six cascaded "And" gates degraded the signal level 0.1 volt.

There are some deficiencies in the system. Pulse "And" gates require a two microsecond gate enable time and a four microsecond gate disable time. D.C. "And" gates will pass a positive pulse even though they have a "0" on the other inputs. These circuit characteristics may cause trouble in some instances. These deficiencies were the only serious ones noted in familiarization with the equipment.

This equipment has extensive possibilities for expansion and development. The equipment would be useful in illustrating concepts involved in all types of pulse circuitry. It could be used for a logical extension of the present digital computer circuits course. There is no theoretical limit as to how many of these Bread Boards can be connected together. Thus it is conceivable that an entire computer could be made from this equipment including input/output equipment and a memory.

Included as Appendix C is a catalog of all the available units that can be used with this Bread Board. The catalog include all technical specifications of the equipment.

III. Preparation of Experiments

General

The largest part of this thesis, from a standpoint of work expended, was in the preparation of some ten experiments. These experiments are included in the appendix as Appendix A. The titles of these experiments are listed in Table II.

Table II

List of Experiments

Experiment Number	Title
EE-309-1	Coding (Problem Drill)
EE-309-2	Equipment Familiarization
EE-309-3	Boolean Algebra
EE-309-4	Logical Construction (Full and Half Adders)
EE-309-5	NOR-NAND Logic
EE-309-6	Shift Registers
EE-309-7	Counters
EE-309-8	Pulse Train Generators and Complementers
EE-309-9	Arithmetic Logic
EE-309-10	Logic Design

The experiments were written using the following assumptions:

(1.) The experiments will be used to supplement an Electrical Engineering course with the same basic format of EE-309, Digital Computer Circuitry. It is important to note that these experiments must be used in conjunction with a theory course. They are not meant to fully explain the theory of the circuits involved. The theory discussed in each experiment is designed for review purposes only.

(2.) The text, Computer Logic by Ivan Flores, or a text similar to it, will be used in the course. A text was chosen for convenience. Nothing precludes the use of any other text, but some ambiguity of terminology may arise. Flores was chosen on the basis that this was the text that was used the last two times that EE-309 was included in the curriculum. The chronological sequence of experiments and the terminology used is based on Flores's conventions.

(3.) The experiments will be conducted on the Digital Bread Board described previously in this thesis.

(4.) The general approach of the student will be to prepare the logic diagrams prior to coming to the laboratory. Should he wait until he comes to the laboratory to construct the diagrams, he probably will not finish the experiments in the time allotted.

In so far as was possible, these experiments have been performed to determine their feasibility on the Bread Board. Comments on the individual experiments will be made in this chapter in the next section. The available equipment included only one inverter and one delay. As several of these devices are essential in the design of many logic circuits, it was impossible to perform all the experiments. Other experiments required more equipment than was available, so could not be performed.

An instructor teaching this laboratory course should work all experiments prior to giving them to the students. There are some

minor points that are not readily apparent to the new student. There is no substitute for familiarization with the equipment.

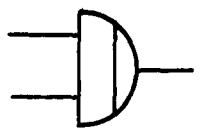
One important subject that may have been under emphasized in the experiments is the subject of coders and decoders. Circuit realization of these devices require extensive use of "And" gates. Enough "And" gates to perform these functions may not be available under all circumstances to perform experiments using these devices. The logic of these devices is not difficult to understand; therefore, their exclusion does not unduly detract from the experiments.

The logic symbols that will be used in this thesis are given in Fig. 3 and are consistent with Flores's convention.

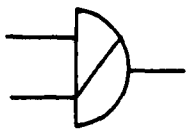
Experiments

Coding. One of the first subjects discussed in Flores is the subject of coding. This is not in any way designed to take the place of a formal course in digital computer programming. It is intended to give the student of logic design a basic understanding of some of the problems that the computer must solve. The only way that one can learn these basic premises is by practice. This Problem Drill is intended to give the instructor the opportunity to discuss the problems presented in the drill as well as other points germane to coding problems.

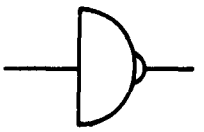
Equipment Familiarization. In general, students will have no previous experience in using digital equipment. It would be next to impossible for him to perform experiments and at the same time



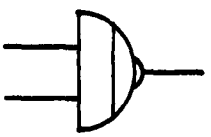
"And"



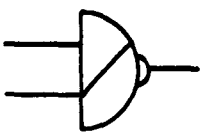
"Or"



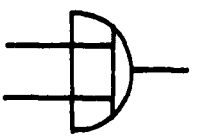
Not
(Inverter)



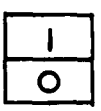
"Nand"



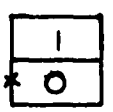
"Nor"



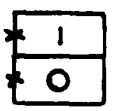
"Exclusive Or"



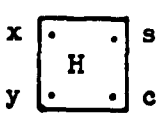
Flip Flop



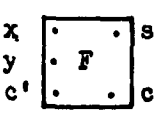
Univibrator



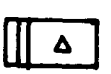
Astable
Multivibrator



Half Adder



Full Adder



Delay

Figure III
Logic Symbols

become familiar with the equipment. The experiment discusses in some detail each type of logic circuit that will be used in the remaining experiments.

Boolean Algegra. This experiment is designed to demonstrate how the solution of Boolean equations can be solved using electronic equipment. There is also practice given in solution of Boolean equations using algebra laws, Karnaugh Maps, and truth tables. As this experiment requires the extensive use of "Not" elements, this experiment has not been realized on the Bread Board. It is simple D.C. logic and should offer no difficulties.

Logical Construction (Full and Half Adders). Construction of a device that will fulfill the requirements of the addition truth table is a logical initial approach to realization of logic functions. The experiment has been performed without difficulty.

NOR-NAND Logic. This experiment explores some of the characteristics of some different truth propositions. An algorithm for the conversion of And-Or logic to Nor-Nand logic is developed and discussed (Ref 1:1-2). For the purpose of this experiment a "Nor" gate is realized by placing an inverter on the output of the "Or" gate, and a "Nand" gate is realized by placing the inverter on the output of an "And" gate. This experiment requires the extensive use of inverters and was not performed. This experiment is straight-forward and should not be difficult. No proof is offered for the algorithm presented in the experiment. It appears to work without exception.

Shift Registers. This experiment explains the use of a shift register element that is complete within itself, as well as the development of the shift register element from simple logic building blocks. The first part of the experiment concerns the use of the complete shift register unit. Detailed instructions are given. The second part of the experiment is concerned with the development of the shift register from logic units. The complete experiment has not been performed because insufficient delays were available. If extreme care is used in constructing the shift register, the logic will work.

Counters. This experiment discusses the various ways that logic circuits can be made to indicate the number of input pulses. This experiment has been performed in its entirety and is realizable on the Bread Board. The problem of the race condition becomes apparent in the design of the foreshortened counter. Pulse "And" gates must be used in some instances.

Pulse Train Generators and Complementers. This experiment developes the characteristics of pulse train generators and complementers. There is no particular reason for these two subjects to be put together except that neither subject is long enough to warrant an individual experiment, and both are important enough to include in the experiments. The pulse train generator part has been accomplished. Again the lack of inverters prevented realization of the complementing part of the experiment. This

experiment is long and will definitely require outside preparation of the student in order for him to complete the experiment in the required time.

Arithmetic Logic. This experiment is the first chance for the student to realize a complete functional unit. He must design and build a device that will take two natural binary coded numbers, add them, and store the sum in a predetermined place. The logic is reasonably direct; however, due to equipment shortage it was not possible to implement this design on the Bread Board. It is recommended that the instructor determine whether the included solution is indeed feasible. The race condition in this problem will be quite severe.

Logic Design. This experiment gives the student opportunity to further develop his capability to solve complete logic problems. The experiment is designed to demonstrate the student's ability to apply his acquired knowledge in logic to a circuit other than a digital computer circuit. The logic of these problems is direct; their realization may not be. Again this experiment was not performed due to equipment shortage.

IV. Cost Analysis

The cost of any system depends on the capability of the system. This fact will hold true for the cost to realize the digital laboratory capability. It is assumed that it is desirable to have the student do as much individual work as possible. This equipment is not inexpensive, so a compromise must be reached.

The cost of the equipment required to perform the experiments is derived in Appendix B. It is assumed that a desired maximum of two people would work on any one Bread Board at one time. The problem then resolves itself into one of how much money is available to be spent.

For $4526.95, it is possible to obtain the capability to have two separate groups of two working on Experiments 2 through 8 and one large group working on Experiment 9 or 10.

For $8878.00, it is possible to double the laboratory capability. It should be observed that the cost per unit is not constant but decreases as more units of one type are purchased. This would tend to discourage gradual purchase of the units. (Ref 12:1-10).

V. Recommendations

Analysis of the problem of realization of a digital computer laboratory capability has been completed. It is certainly financially and electronically feasible to realize this capability. The main obstacle is the source of funds to finance this venture. This problem is not considered within the scope of this thesis.

It is strongly recommended that immediate steps be taken to obtain the necessary equipment to establish the laboratory. Minimum equipment required would be enough to obtain the capability for four groups to work concurrently. It was developed in Chapter IV that this capability would cost $8878.00.

There are two logical extensions of this thesis.

(1.) Time did not permit analysis of the cost in money and labor to locally design and manufacture a digital trainer. Should the funds to finance purchase of the bread board be withheld, it might be worthwhile to investigate the possibility of building the trainer within the resources of the Institute.

(2.) There is no reason that a complete digital computer can not be built using these Bread Boards. It is conceivably worthwhile to undertake the project of designing a small computer complete with memory using these Bread Boards. The design would include a cost estimate. The magnitude of this task is not immediately apparent.

Bibliography

1. "A Convenient Method of Implementing Logic with NOR Circuits." Digitimes, 1:1-2 (No date).

2. Digital Building Blocks for Electronics Equipment and Systems. Advertising catalog. Santa Ana, California: Engineered Electronics Company, 1961.

3. Digital Modules. Advertising brochure. Maynard, Massachusetts: Digital Equipment Corporation (No date).

4. Digital Test Equipment 3000 Series. Advertising brochure. Maynard, Massachusetts: Digital Equipment Corporation (No date).

5. EECo Digital Circuits Modules Catalog. Equipment catalog. Santa Ana, California: Engineered Electronics Company (No date).

6. Flores, Ivan. Computer Logic. Englewood, New Jersey: Prentice Hall, 1962.

7. Hohn, Franz E. Applied Boolean Algebra, An Elementary Introduction. New York: The Macmillan Company, 1960.

8. Programmable Digital Training Systems Series PE 1. Advertising brochure. Natick, Massachusetts: Control Logic Incorporated (No date).

9. Pro-Log. Advertising brochure. Dayton: Jackson Electrical Instruments (No date).

10. Series PE 1 Programmable Equipment. Advertising brochure. Natick, Massachusetts: Control Logic Incorporated (No date).

11. Siegal, Paul. Understanding Digital Computers. New York: John Wiley and Sons Incorporated, 1961.

12. T-Series Price List. Advertising catalog. Santa Ana, California: Engineered Electronics Company, 1962.

13. Univac Digital Trainer. Advertising brochure. St. Paul: Univac Division of Sperry Rand Corporation (No date).

14. Welded Digital Circuits. Shortform catalog. Natick, Massachusetts: Control Logic Incorporated (No date).

Appendix A

Laboratory Experiments

AIR FORCE INSTITUTE OF TECHNOLOGY

Department of Electrical Engineering

Laboratory Experiment No. EE-309-1

A. TITLE: Coding (Problem Drill)

B. PURPOSE: To demonstrate some simple coding problems and to enhance the student's familiarity with coding by use of a simple problem drill.

C. DISCUSSION:

I. Preliminary: This drill is not intended to fulfill the requirements of a digital computer programing course; but, rather, is intended to acquaint the student of computer logic with the basic functions of the computer. In order to define the instructions to be used, this drill has been prepared for use with Ivan Flore's book Computer Logic Prentice-Hall Inc., Englewood, New Jersey III (1962). However, nothing is to prevent the instructor or student from defining his own processes and using the problems for illustrative examples. It is not intended to introduce the concept of cycle and index registers as this would tend to obscure the main thought of the iteritive process.

II. Coding: The following coding will be used. If the instructor or student prefers, he may substitute other codes as long as the purpose of the problems is not obscured.

a. ADD: (A) + (M) → A Add the contents of the designated memory location (a three digit number) to the number in the A register and store the sum in the A register.

b. SUB: (A) - (M) → A Subtract contents of M from A and store in A

c. MUL: (M) X (L) +(A) → A ⌣ L Multiply contents of L register by M, add product to A register, and store in the A augmented L register.

d. DIV: (A)/(M) → Q, Remainder → A Divide contents of A by contents of M and store the quotient in Q with the remainder in A.

e. XAM: ( ) ( )
XMA
XLM
XML
XQM
XMQ
Transfer contents of second term to the third term. (Notice that in this case, Flores has been expanded and there are additional transfers allowed).

XAL

XLA

XQA

XAQ

f. CMP: (A):( ) Compare contents of A register with contents of a designated memory location.

g. JOP: (A)>(M')→M
(A)≯(M')→I+1 If A greater than some previous compared value (M'), jump to some new instruction located in location M. If A not greater than M', then proceed to the next instruction.

h. JOM: (A)<(M')→M
(A)≮(M')→I+1 If A less than some previous compared value (M'), jump to some new instruction located in location M. If A not less than M', proceed to the next instruction.

i. JOE: (A) = (M')→M
(A) ≠ (M')→I+1 If A is equal to some previous compared value (M'), jump to some new instruction located in location M. If A is not equal to M', proceed to next instruction.

j. UCJ: → M Proceed to location M.

k. STP: Stop.
(Ref 6:76)

III. The Machine: It is assumed that the machine that will be illustrated by this drill will be the fictional Polyvac described by Flores. For the purpose of this drill the following specifications are enumerated (Ref 6:152):

a. Word length --------Nine decimal characters plus sign

b. Instruction---------First three characters of word

c. Operand ------------Second three characters of word

d. Memory ------------One thousand word memory with locations 000 through 999

e. Instruction -------Single address

Other specifications can be found in Computer Logic by Ivan Flores, Prentice-Hall, Inc., Inglewood, New Jersey, III, (1962).

D. DRILL: The following data will be used in the problems:

I. The index i will vary from 0 to 99 unless otherwise indicated in the problem.

II. The computer will always go to memory location 000 at the beginning of operation.

III. The computer will not stop unless it is told to do so.

IV. a. Data Ai is stored in locations 100+i up to location 199.

b. Data Bi is stored in locations 200+i up to location 299.

c. Data Ci is stored in locations 300+i up to location 399.

d. Data Di is stored in locations 400+i up to location 499.

e. Data Ei is stored in locations 500+i up to location 599.

E. PROBLEMS: Solve each of the following problems by making flow diagrams and then coding the necessary steps.

I. Ci - Ei ----------600+i

II. Ai + Bi ----------700+i (i varies between 0 and 49)

Ai - Bi ----------800-i (i varies between 50 and 99)

III. $\frac{AiBi - Ei}{Ci}$ --------600+i

IV. Devise a routine that will solve the areas of circles whose radii are stored in location Bi and store the result in 700 + i. (If is is necessary to use any additional information, indicate the location of the information in the memory.)

V. The sides of a rectangle Ri are stored in locations Bi and Ci. Determine the rectangle whose area is the largest. Place the number of the rectangle in 700 and its area in 701.

VI. Compare the data in Ci and Di. If Ci is greater than Di, store the difference in 700 + i and Ci in 600 + i. If Di is greater than Ci, store the difference in 900 + i and Di in 800 + i. If at any time Ci equals Di, store Ci in 100, store Di in 101, and stop.

F. REFERENCE:

I. Flores, Ivan. Computer Logic. Englewood, New Jersey: Prentice-Hall Inc., 1960.

AIR FORCE INSTITUTE OF TECHNOLOGY

Department of Electrical Engineering

Laboratory Experiment No. EE-309-2

A. TITLE: Equipment Familiarization

B. PURPOSE: To acquaint the student with the capabilities and limitations of the EECo Digital Bread Board.

C. DISCUSSION: No report will be required from this experiment. The theory of each circuit will be discussed to the extent required in the procedure part of the experiment.

D. EQUIPMENT:

I. Digital Bread Board

II. Oscilloscope (Dual beam)

III. VTVM

IV. 1 4 Input "And" Gate

V. 1 4 Input "Or" Gate

VI. 1 Flip Flop

VII. 1 Univibrator

VIII. 1 Astable Multivibrator

IX. 1 Pulse "And" Gate

X. 1 Pulse "Or" Gate

XI. 1 Inverter

XII. 1 Emitter Follow

XIII. 1 "Exclusive Or" Gate

E. PROCEDURE:

I. General

a. The equipment has two states, "1" and "0". The "1" state is represented by -3 volts, and the "0" state is represented by -11 volts. This convention will hold true throughout these experiments. There are other voltages available in the system, but these are for use in the circuit function and are not of interest in this course. The state voltages are available on the board as will be shown presently.

b. Notice that each banana jack has its own distinct color. Measure the voltage in the light blue jack with the VTVM. Are the light blue jacks "1" or "0"? Repeat for the dark green jacks._____.

c. Notice the eight 9-pin and eight 13-pin sockets arranged in three (four) horizontal rows. One of each type is located over alternating white and blue banana jack. These sockets are the receptacles for the nine and thirteen pin logic units respectively. It is important to note that only one of the two receptacles can be used at one time.

d. Below each of the sockets, there are rows of lights and binding posts. These lights will indicate the state of an input that is put into it. Indicate which state lights the light._____ The binding posts may be used for the attachment of external

parts such as capacitors or resistors.

e. At the top of the board is the signal generator panel. At the extreme right is the D.C. reset button with one output marked Flip Flops and the other marked Decades. The Flip Flop output will be used in this experiment to reset flip flops. Pushing this button will ground the output. Next to the D.C. reset is a series of lights. These lights and their banana jacks are used for inserting "1's" and "0's" in the logic circuit. Determine when the light is lit.____ Next to the lights are sockets for two logic elements. These are sockets for pulse generators. The buttons to the immediate left of the sockets will produce a single positive going pulse from their respective output jacks. On the left part of the board is an astable multivibrator used for generating pulse trains. Next to the socket is a five position rotary for determining frequency of the multivibrator. Confirm that the two outputs of the multivibrator are 180 degrees out of phase. (A dual beam oscilloscope is required. This part may be omitted at the discretion of the instructor.)

f. Insert into a socket a 4 input "And" gate. Be sure that care is taken in putting the logic device into the socket to preclude bending the pins. Connect

appropriate logic card on the board. Note that shorts are required. These particular 4 inputs gates can be converted into two 2 input "And" gates by making the appropriate connections on the logic card. Connect the gate in the 4 input mode. Take data to fill out the logic truth table below.

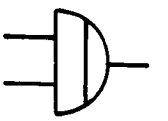


Figure 1
DC And Gate

AND Truth Table

A	B	C	D	&
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Figure 2

Verify to your own satisfaction that the circuit works according to the AND logic when connected as a dual 2 "And" gate.

g. Connect the logic device and card for a 4 input "Or" gate. Connect the circuit for a dual 2 input "Or" gate. Connect output of one of the gates to a light. Connect the inputs to appropriate voltage levels to fill out the truth table below.

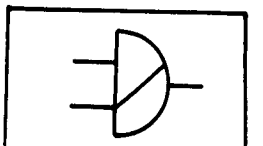


Figure 3
DC Or Gate

OR Truth Table

A	B	v
0	0	0
0	1	1
1	0	1
1	1	1

Figure 4

h. Connect a flip flop. Connect one of the outputs to one indicator light and the other output to another light. Note that only one of the lights is lit at one time, but that one light is lit at all times. Use the manual trigger and the DC reset button to determine the function and required input of the following indicated input positions:

1. Trigger-------
2. DC Reset------
3. AC Reset------
4. AC Set--------

i. Connect the univibrator. What state is the "uni" without an input._____. The

following equations determine the required capacitance to produce a certain delay.

(T-166) $Cx = 60(T-2)$ (1)

(T-167) $Cx = 100(T-2)$ (2)

T in Usec.
Cx in uuf

Connect a .1 uf capacitor between pins 2 and 3. Connect the manual pulse generator to the AC trigger input. Determine the delay of the univibrator with use of a dual trace oscilloscope._____. How does this compare with the theoretical delay?_____

j. Connect a pulse "And" gate to the circuit. Connect the output of the Pulse "And" gate to the trigger input of a flip flop. Connect the output of one side of the flip flop to an indicator light to determine when the pulse "And" gate produces an output. Take the necessary data to determine the output logic of this gate.

k. Repeat the prodedure for part j. above using a pulse "Or" gate instead of the pulse "And" gate.

l. Connect an inverter to the bread board and take the data to verify the truth table below.

NOT Truth Table

A	$\bar{A}$
0	1
1	0

Figure 5

m. Connect an emitter follower to the bread board. Verify that the output of the emitter follow is in phase with the input. The emitter follow is not a logic device in the true sense of the word. It does serve an extremely useful purpose when connected to the output of logic devices. The emitter follower perserves the voltage levels, and it gives the logic device increased capability to drive logic circuits without excessive loading. The "And" and "Or" gates are provided with internal emitter followers and seldom will need the "assistance" of an emitter follower. In cases where loading becomes severe on flip flops, it may become necessary to use emitter followers to prevent degradation of the signal levels.

n. Next connect an "Exclusive Or" gate to the board. Complete the truth table below.

Exclusive Or Truth Table

A	B	A⊕B
0	0	
0	1	
1	0	
1	1	

Figure 6

F. COMMENTS:

I. The logic circuits that are described above are not the only ones that are available in this series. A few will be introduced in the various laboratory experiments; others will not be discussed at all. Complete description of all circuits is available in the reference.

II. Each student should insure that he keeps this circuit description available throughout the course as the subject matter covered here will not be repeated in the succeeding experiments.

III. This digital bread board is almost impervious to breakage; however, some basic precautions should be perserved.

a. Use care in inserting logic devices into sockets. Do not force them.

b. Use VTVM for all voltage measurement.

c. Should the protective shield come off of the device, shut down the equipment and call your instructor.

G. REFERENCES:

I. Flores, Ivan. Computer Logic. Englewood, New Jersey: Prentice-Hall Inc., 1960.

II. EECo Digital Circuit Modules Catalog T72. Advertising catalog. Santa Ana, California: Engineered Electronics Company, n.d.

AIR FORCE INSTITUTE OF TECHNOLOGY

Department of Electrical Engineering

Laboratory Experiment No. EE-309-3

A. TITLE: Boolean Algebra

B. PURPOSE: To study the various properties of Boolean functions and to show the utility of Karnaugh Maps.

C. DISCUSSION:

I. Theory:

a. The theory of Boolean functions will not be approached as an end in itself, but rather as one of several tools that are useful in study and design of digital computers.

b. This experiment will approach three main aspects of the problem: reduction of Boolean functions, truth tables, and Karnaugh Maps. Each problem will attempt to demonstrate the importance of these approaches for ultimate problem solution.

II. Boolean Algebra Laws:

a. Commutativity

$$A + B = B + A$$
and
$$(A)(B) = (B)(A)$$

b. Associativity

$$(A+B) + C = A + (B+C)$$
and
$$(AB)C = A(BC)$$

c. Distributivity

$$A(B + C) = AB + AC$$
and
$$A + BC = (A + B)(A + C)$$

d. Null Elements

$$A + \Lambda = A$$
and
$$A\Lambda = \Lambda$$

e. All Elements

$$A + I = I$$
and
$$AI = A$$

f. Not Elements

$$A + \bar{A} = I$$
and
$$A\bar{A} = \Lambda$$
and
$$\bar{\bar{A}} = A$$

g. De Morgan's Law

$$\overline{AB} = \bar{A} + \bar{B}$$
and
$$\overline{A + B} = \bar{A}\,\bar{B}$$

III. Truth Tables: One method of defining the logic of a particular function is by truth tables. Three of the truth tables find particular use in adapting to analysis of digital circuits and follow the rules of Boolean Algebra.

a. Truth table for "And" (&) or (.)

A	B	A&B
0	0	0
0	1	0
1	0	0
1	1	1

b. Truth table for "Or" (V) or (+)

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

c. Truth table for "Not" ($\bar{}$)

A	$\bar{A}$
0	1
1	0

IV. Karnaugh Maps: Another useful tool for analysis and simplification of Boolean functions is Karnaugh Maps. Their utility will be demonstrated during this experiment. For a detailed description on theory, consult the references at the end of the experiment.

D. EQUIPMENT:

I. Digital Bread Board
II. Oscilloscope
III. VTVM
IV. 4 "Not" Gates
V. 3 3 Input "And" Gates
VI. 3 2 Input "Or" Gates

E. PROCEDURES:

I. Using equipment available, take necessary data using VTVM to prove truth tables given in part C, III.

II. Prove using Boolean Algebra that the following expression is true:

$$(X + Y)(X + \overline{Y}) = X$$

III. Repeat (II) above first using truth tables and then using Karnaugh Maps. Draw "D" box diagram and take necessary data to prove validity of the expression.

IV. Simplify the following expression using De Morgan's Laws:

$$\overline{(\overline{X} + \overline{Y})}X + \overline{\overline{X}\,\overline{Y}}$$

V. Verify (IV) by using Karnaugh Map simplification. Draw "D" box diagram and take necessary data to verify the problem

VI. Simplify first by Boolean Algebra and second by Karnaugh Maps. Show that the two solutions are equal.

$$X\,Y\,Z + \overline{X}\,\overline{Y}\,Z + \overline{X}\,\overline{Y} + \overline{X\,Y\,\overline{Z}}$$

VII. Use the truth table to prove that the following statement is true:

$$\overline{X}\overline{Y} + X = I$$

X	Y	X Y	$\overline{X}\overline{Y}$	$\overline{\overline{X}\overline{Y}} + X$
0	0			
0	1			
1	0			
1	1			

VIII. Prove by use of the equipment provided that the output is always "1" regardless of the input.

IX. Show first by Boolean Algebra and second by Karnaugh Maps that the following expression is true:

$$(X + Y)(\overline{Y} + Z) = Y Z + X \overline{Y}$$

X. Draw "D" box diagram and necessary data to verify IX.

F. REPORT:

I. Perform the operations required in part E.

II. Simplify the following Boolean equations using Boolean Algebra:

a. $\overline{A}\,C\,D + \overline{A}\,B\,D + B\,\overline{C}\,D + \overline{A}\,C\,D + B(\overline{A\,C})D + \overline{A}\,C\,\overline{D} + B(\overline{A\,C})\overline{D}$

b. $W\,\overline{Y}\,Z + \overline{W}\,X\,\overline{Y}\,Z + \overline{W}\,\overline{X}\,\overline{Y}\,Z + W\,X\,Y\,Z + \overline{W}\,\overline{X}\,\overline{Y}\,\overline{Z} + W\,\overline{X}\,Y\,Z + \overline{W}\,\overline{X}\,Y\,\overline{Z}$

c. $\overline{\overline{X}\,\overline{Y}}(\overline{X}\,\overline{Y} + X\,Y) + X\,Y$

d. $(\overline{X} + \overline{Y})(\overline{X\,Y}) + X\,Y(X + Y)$

e. $A\,B\,C(\overline{A}\,C + \overline{B}\,\overline{C}) + \overline{A}\,\overline{B}\,\overline{C}(A\,B + \overline{B}\,C)$

III. Repeat II using Karnaugh Maps.

IV. Prove the generalized version of De Morgan's Laws for n variables.

V. The truth tables that we have discussed so far have been concerned with three truth tables- "And", "Or", and "Not". Suppose that it is necessary to use a truth table as indicated below:

X	Y	
0	0	0
0	1	1
1	0	0
1	1	0

Write the defining equations and draw a "D" box diagram.

VI. Repeat V above for the "Exclusive Or" function given below:

X	Y	X ● Y
0	0	0
0	1	1
1	0	1
1	1	0

G. REFERENCES

I. Flores, Ivan, Computer Logic Englewood, New Jersey; Prentice-Hall Inc., 1960.

II. Hohn, Franz E. Applied Boolean Algebra, An Elementary Introduction. New York: The Macmillan Co., 1960.

AIR FORCE INSTITUTE OF TECHNOLOGY

Department of Electrical Engineering

Laboratory Experiment No. EE-309-4

A. TITLE: Logical Construction (Full and Half Adders)

B. PURPOSE: To study the logical construction and characteristics of full and half adders and to build, by use of logical elements, circuits that will perform the required functions of these devices.

C. DISCUSSION:

I. Theory:

a. One of the vital functions that takes place in any computer is the arithmetic function. A necessary operation that must be carried out in this function is the performance of binary addition and/or subtraction. Making use of the similar properties of Boolean algebra manipulation and digital arithmetic, we can formulate circuits that will perform the required functions.

b. The half adder will be the first approach to fulfilling the arithmetic requirements. Further development will follow showing a natural progression to more complicated devices.

c. The use of Boolean algebra becomes an important tool in optimizing circuit design. The use of truth tables

is essential in determining formulation of Boolean equations to represent the logic function.

II. Definition:

a. Half Adder. A half adder is a device that will perform binary addition by taking an "X" input (the) Augend) and a "Y" input (the Addend) and produces two outputs the Sum and Carry. Symbolic characterization of the half adder is shown below.

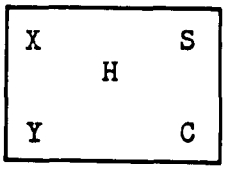


Figure 1

b. Full Adder. A full adder is a device that will perform binary addition by accepting three inputs- an "X" input (the Augend),a "Y" input (the Addend), and a Carry digit C', (from a preceding addition) and producing two outputs- the Sum and the Carry. Symbolic characterization of the full adder is shown below.

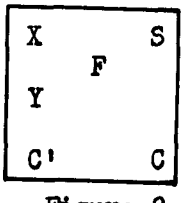


Figure 2

D. EQUIPMENT:

I. Digital Bread Board
II. Oscilloscope
III. HP VTVM
IV. 4 "Not" Gates
V. 6 2 input "And" Gates
VI. 3 2 input "Or" Gates
VII. 2 Half Adders (Optional)

E. PROCEDURE:

I.

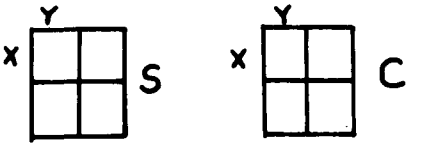
a. Using standard notation with "X" (the Augend) and "Y" (the Addend), complete the truth table for binary addition shown below:

X	Y	C	S

b. Write the Boolean equations for Sum and Carry in their most simple form. Use Karnaugh Maps.

S =

C =



S =

C =

c. Draw "D" box diagram for half adder indicating inputs and outputs.

d. Take measurements using VTVM of outputs to verify truth table for all possible inputs.

II.

a. As in Part I, A., above construct a truth table for a full adder using for inputs "X", "Y", and "C'" and "C" and "S" as the outputs.

X	Y	C'	S	C

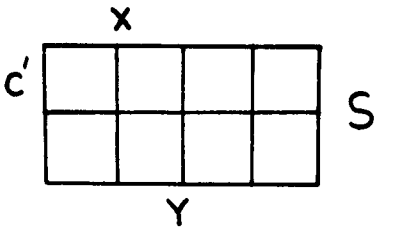
b. The approach to obtain a full adder might be to connect in series two half adders. Successive application of the equations derived in Part I can then be used to obtain the necessary outputs that will satisfy the truth table for the full adder. Show first, by successive series connection of two half adders and then second, by "D" box diagram, how a full adder may be constructed using this approach to solve the problem.

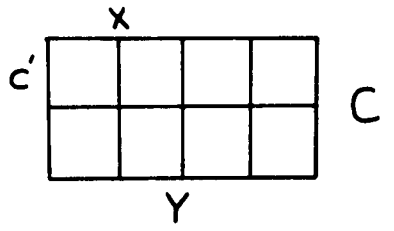
c. Construct full adder obtained above and take necessary readings with a VTVM to verify truth table. (Note! Direct use of half adder modules may be used if sufficient simple logic elements are not available.)

d. Write Boolean equations for full adder. Simplify using Karnaugh Maps.

S =

C =





S =

C =

e. Draw a "D" box diagram of full adder using equations above. Construct full adder using logic devices and obtain necessary VTVM readings to verify truth table.

F. REPORT:

I. Perform the operations required in Part E.

II. Compare the "D" box diagrams of Part E, II, b, with the diagram in Part E, II, e. How many logic elements are saved by the second method? Construct "D" box diagram for full adder from original defining equations. Compare with diagram constructed in Part E, II, e.

III. Show by a diagram how a half adder can be constructed using mechanical switches. Repeat using a full adder.

IV. This experiment has emphasized the use of the addition function. A similar derivation can be made using subtraction. Construct a truth table for a half

subtractor ignoring the possibility of a borrow term originating from the previous subtraction. Be sure to specify which variable is the minuend and which is the subtrahend. Repeat this procedure for a full subtractor, this time considering the possibility of a borrow prime term originating from the previous subtraction. Write the defining equations and simplify using Karnaugh Maps. Compare the resulting "D" box diagram with that diagram in Part E, II, e.

AIR FORCE INSTITUTE OF TECHNOLOGY

Department of Electrical Engineering

Laboratory Experiment No. EE-309-5

A. TITLE: NOR-NAND Logic

B. PURPOSE: To study some of the characteristics of NOR-NAND logic circuits and to develop some tools that are useful in converting conventional logic expressions into NOR-NAND logic diagrams.

C. DISCUSSION:

I. NOR logic is defined as the inverse of OR logic

Truth Table

A	B	OR	NOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Figure 1

Expressing this in equation form, it is found that

$$A \| B = \overline{A + B} \tag{1}$$

(The convention that will be used in this experiment to denote the NOR and NAND functions will be those used by Franz E. Hohn in his book Applied Boolean Algebra, An Elementary Introduction.) (Ref. 7:56)

Other useful identies are the following:

$$A \| A = \overline{A} \tag{2}$$

$$\overline{A} \| \overline{B} = AB = (A \| A) \| (B \| B) \tag{3}$$

$$\overline{A \| B} = A + B = (A \| B) \| (A \| B) \tag{4}$$

II. NAND logic is defined as the inverse of AND logic.

Truth Table

A	B	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Figure 2

Expressing this in equation form, it is found that

$$A \mid B = \overline{AB} = \overline{A} + \overline{B}$$

III. The use of these logic functions is increasing in popularity. From an electrical engineering viewpoint, is is possible to make the same circuit perform both functions merely by changing the assignment of logic levels. (Ref 2: Pages unnumbered) Thus it becomes theoretically possible to build entire logic systems using one type of circuit. It is even possible to build storage elements and univibrators (with some minor additions) using these elements. (Ref 6:159).

IV. Engineered Electronics Company of Santa Ana, California, can take credit for development of a simple algorithm to convert normal logic statements into NOR-NAND logic diagrams (Ref 1:1). Basically it consists of four parts.

a. The conventional equation must not consist of multi-variable not functions. These must be converted to

single variable not function. (Example: The function $\overline{A + B + C}$ must be simplified to $\bar{A}\,\bar{B}\,\bar{C}$.)

b. The simplified logic expression must be converted into a conventional logic diagram keeping in mind that cascaded "AND" and "Or" gates must be converted into single gates. (i.e. one "AND" (OR) gate can not drive another like unit.)

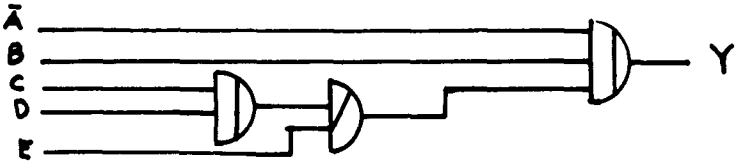
c. Using NAND-NOR representation draw the circuit again in the exact form as in (b.). If the output of the original expression was taken from an "And" gate, NOR logic will be used. If the output was taken from an "Or" gate, NAND logic will be used.

d. The final step is to count the number of gates between the output and each input. If the number of gates is even, then the input is left exactly as it was. If the number of gates is odd, then the input should be changed at that point to its inverse.

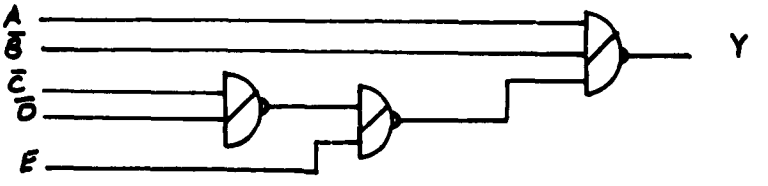
V. The following example will demonstrate the manner in which this procedure can be used. Take the expression $Y = A.B(CD + E)$.

a. Notice that this expression does not contain any multivariable not functions.

b. Draw the conventional logic diagram.



c. Notice that the output from the original diagram came from an "And" gate. Therefore, the circuit takes the form or a NOR logic diagram using "NOR" gates. Draw the same diagram using "NOR" gates, but do not put the input signals on at this time.



d. Count the number of gates between the output and each input. If the number of gates is even, then mark the input exactly the same as the input in the original logic diagram. If the number is odd, mark the gate the inverse of what it was in the original diagram. Notice that in the resultant NOR-NAND circuit $\bar{A}$, B, C, and D are changed to A, $\bar{B}$, $\bar{C}$, and $\bar{D}$.

D. EQUIPMENT:

I. Digital Bread Board
II. VTVM
III. 1 3 Input "And" Gate
IV. 3 2 Input "Or" Gate
V. 1 3 Input "Or" Gate
VI. 5 Inverters

E. PROCEDURE:

I. Construct a truth table to show that the NOR circuit

derived in the example of Part C, V, is valid.

II. Synthesize the logic circuit of Part I above and take the necessary data to verify the circuit. (For "NOR" gates, use an "Or" gate followed by an inverter. For "NAND" gates, use an "And" gate followed by an inverter.)

III. Convert the following Boolean expressions to NOR-NAND circuits using the procedure outlined in Part C.

a. $X = A + BC(D + E)$

1. Conventional logic diagram:

2. NOR-NAND diagram:

b. $Y = A + B + CD$

1. Conventional logic diagram:

2. NOR-NAND diagram:

IV. Build the two NOR-NAND logic circuits derived in Part III above and take the necessary data to verify your diagrams.

V. Construct a truth table for a half adder.

A	B	Sum	C
0	0		
0	1		
1	0		
1	1		

VI. Write the Boolean expressions for the Sum and Carry for a half adder.

Sum =

Carry =

VII. Convert the expressions above to NOR-NAND circuits and take data to verify your results. (Use inverters when you have a one input "NOR" or "NAND" gate.)

F. REPORT:

I. Perform the experiment as required in Part E.

II. Prove by use of truth tables Equations (3) and (4).

III. Using the identities in Part C, derive the expressions for Sum and Carry of the Half Adder. Do the results of Part E, VII, confirm these derivations?

IV. Using the identities, convert the following expressions to NOR logic.

a. $X = \overline{AB} + AB$

b. $Y = A(B + \overline{C}) + C$

c. $X = AB + BC + \overline{AC}$

V. Using the procedure in Part C, IV, convert the following expressions to NOR-NAND logic diagrams.

a. $X = (A + B) + (BC + \overline{D})$

b. $Y = A\overline{B}(\overline{BC} + D)$

c. $X = (\overline{A + B}) + C + D$

D. REFERENCES:

I. Flores, Ivan. Computer Logic. Englewood, New Jersey: Prentice-Hall, Inc.,

II. Hohn, Franz E.. Applied Boolean Algebra, An Elementary Introduction. New York: The Macmillan Co., 1960.

III. Siegal, Paul. Understanding Digital Computers. New York: John Wiley And Sons Inc., 1961.

AIR FORCE INSTITUTE OF TECHNOLOGY

Department of Electrical Engineering

Laboratory Experiment No. EE-309-6

A. TITLE: Shift Registers

B. PURPOSE: To illustrate some of the important characteristics of shift register elements and to demonstrate some of the various methods for constructing these devices.

C. DISCUSSION:

I. A shift register is a logic device composed of a series of bit storage elements and the necessary gating circuitry to move the bits from one storage element to another in some predetermined fashion. The bits must be moved simultaneously and must not interfere with each other (Ref 6:162). There are many ways that this register can be constructed. The storage devices may be distinct or they may be built into the circuit. This experiment will discuss both types.

II. The first type of circuit that will be discussed is the shift register with the built in storage capability. These shift registers have the shift capability of series in, series out; or parallel in, series out. Distinct pulse must be applied at the appropriate point to gate in the DC value. These devices will be discussed in some detail in Part E.

IV. Another approach to the construction of shift registers is the use of flip flops as bit storage units and pulse gates and delays as the transfer elements. Again these types of shift registers can have whatever input/output characteristic desired.

D. EQUIPMENT:

I. Digital Bread Board
II. Dual Trace Oscilloscope
III. VTVM
IV. 4 Shift Register Elements
V. 4 Flip Flops
VI. 3 2 Input Pulse "And" Gates
VII. 3 Univibrators

E. PROCEDURE:

I.

a. Connect a shift register element to the board and connect a lead from one state to an indicator light.

b. Inputs numbered 2, 3, and 4 are used to shift serial data into the register. A shift pulse must be applied to pin 4 and at the same time there must be a DC (or coincidental pulse) applied at the appropriate shift data input pin. The best way to avoid confusion in explaining the device is to explain the manner in which a "1" or a "0" would be serially input to the device.

1. To insert a "1"

(a) Connect pin 3 to a -3 volt source. Apply a positive going pulse to pin 4; the register

should shift to the "1" state. (If it was in the "1" state prior to the shift pulse, then it will remain in the "1" state.

(b) Pulse the device again and note that the state does not change.

2. To insert a "0"

(a) Connect pin 2 to a -3 volt source. Apply positive going pulse to pin 4; the register should shift to the "0" state.

(b) Pulse the device again and note that the state does not change.

II. Connect another shift register element to the board. Short pin 7 of the first shift register to pin 3 of the second register, and short pin 8 of the first to pin 2 of the second. Apply a pulse to pin 4 of both elements. Describe what happens._____

Apply -3 volts to pins 2 and 3 on alternate pulses to the first register and note what happens. Satisfy yourself that you are familiar with the serial operation of the register.

III. Short pins 11 and 12 together. Apply -3 volts to pin 5 on one register and pin 14 on the other register. Apply a pulse to pin 11 and describe what happens._____

IV. It is important to realize exactly what is happening in the shift register before you can construct complete logic circuits. The shift register will not work if -3 volts

is applied to both sides of the shift register. -3 volts must be applied to the high side of the register in order to shift the device. If you have any questions about operation of the equipment consult your instructor.

V. Connect 4 shift registers together for serial in, serial out operation. Parallel all shift pulse inputs to the register. Apply -3 volts to pin 3 of the first register and apply one shift pulse. Describe what happens._____ Change the -3 volts from pin 3 to pin 2. Apply three pulses and describe what happens._____ Apply one more pulse and note the result.

VI. Connect -3 volts to pins 2 and 14 of the first register, to pin 5 of the second and fourth register, and to pin 14 of the third register. Short together pins 11 and 12 on all registers. Apply a shift pulse to the transfer pins (pin 11 and 12) and describe the result._____ Apply pulse to the shift pulse input jack and note the result. Vary the inputs to the parallel inputs and satisfy yourself that you are familiar with the operation of this type of shift register.

VII. Using elements other than complete shift register units, draw a logic diagram for a three bit shift register.

VIII. Construct the circuit on the bread board and prove that it works. Call your instructor and demonstrate the circuit's feasibility.

F. REPORT:

I. Perform the experiment as required in Part E above.

II. Discuss some of the uses for a shift register.

III. Draw the logic for a shift register that can shift either to the right or to the left. What would be the usefulness of such a device.

IV. Draw an accumulator using functional blocks of a device that will perform serial addition and store the sum in one of the registers.

G. REFERENCES:

I. Flores, Ivan. Computer Logic. Englewood, New Jersey: Prentice-Hall Inc., 1960.

II. EECo Digital Circuit Modules Catalog T72. Advertising catalog. Santa Ana, California: Engineered Electronics Company, n.d.

AIR FORCE INSTITUTE OF TECHNOLOGY

Department of Electrical Engineering

Laboratory Experiment No. EE-309-7

A. TITLE: Counters

B. PURPOSE: To design and study logic circuits that can be used to count to some predetermined number and circuits that can divide a frequency by some preset amount.

C. DISCUSSION:

I. A counter is a logic element that stores digits in such a manner that it is possible to tell the number of input pulses by the states of individual stages. Basically a counter consists of flip flops connected in cascade in such a manner that when it changes from state "1" to state "0" it produces an output pulse to change the state of the following flip flop. Counters are used for a wide variety of purposes.

II. One use of a counter is use as a frequency divider. It can be readily seen how the input pulses can be divided by a factor of 2^n where n is the number of stages. It is often necessary to divide the input pulses by some number other than a factor of 2^n. In order to see how this can be done, refer first to the truth table describing the operation of a four stage counter. A four stage counter will automatically reset itself on pulse 16. (One

output pulse for 2^4 input pulses.) It is required to reset the counter on pulse number 10. If somehow 6 can be added to the counter during the counting operation, the counter will reset on pulse 10. The problem then resolves itself into one of how to add 6 to the counter during the counting operation.

Truth Table for a Four Stage Binary Counter

Input	Flip Flop 1	Flip Flop 2	Flip Flop 3	Flip Flop 4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1
16	0	0	0	0

Figure 1

Whenever numbers are added to the counter, they should be added to stages in state "0". Six can be added to the counter by adding one to the second and third stages. These ones must be added to the counter when the second and third stages are in state "0". Stages two and three are both "0" on pulses 0, 1, 8, and 9. The addition must also take place on some change in the state of one of the stages that occurs only once in the counting process. Flip Flop four changes state on pulse 8. Also at this time stage 2 and stage 3 are in the "0" state and can be set to the "1" state effectively adding 6 to the counter.

III. One disadvantage in using the preceding procedure to divide the frequencies is that the stages do not always indicate the number of input pulses in a direct way. Another type of counter, often called a foreshortened counter, can be made that will always indicate the total number of pulses received and at the same time reset itself on receipt of a preset number of pulses. This can best be done by the following procedures:

a. Gate appropriate inputs to an "and" gate that will disable the "and" gate when one less than the total number of input pulses required is received. The input pulses have to go through the "and gate and hence when the gate is disabled prohibits the pulse

from triggering the counter.

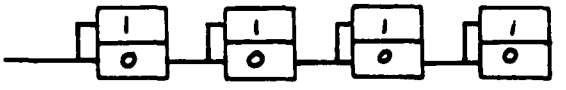
b. When the "and" gate above is disabled, enable another "and" gate which will send the next pulse to the reset trigger of each stage.

D. EQUIPMENT:

I. Digital Bread Board
II. Dual Trace Oscilloscope
III. VTVM
IV. 4 Flip Flops
V. 4 2 Input Pulse "And" Gates
VI. 1 3 Input "And" Gates
VII. 1 Inverter

E. PROCEDURE:

I. Using the diagram below, build a counter.



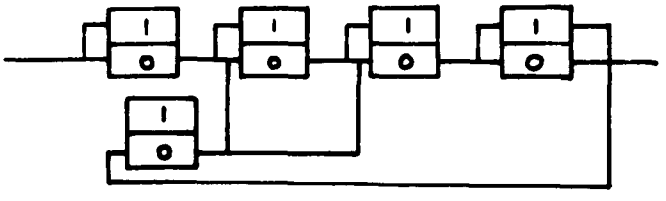
II. Manually step pulses into the counter. Enter the state of each stage in table below.

Input	Flip Flop 1	Flip Flop 2	Flip Flop 3	Flip Flop 4

III. Connect the pulse input to the clock multivibrator set at 5 kc. Using the dual trace oscilloscope, put the

clock pulse on the upper trace and the output of the fourth stage on the lower trace. How many input pulses does it take to get one positive going output pulses? Draw the two waveforms below.

IV. Using the diagram in figure 3 construct a frequency divider.



V. Manually step pulses into the circuit. Enter the state of each stage into the table below. What is the frequency division of this circuit?

Input	Flip Flop 1	Flip Flop 2	Flip Flop 3	Flip Flop 4

VI. Connect the pulse input to the clock multivibrator set at 5 kc. Using the dual trace oscilloscope, put the clock pulse on the upper trace and the output of the fourth stage on the lower trace. Draw the waveforms.

VII. Using the same basic diagram in Figure 3, draw a frequency divider that will divide at a frequency division of 13. What stages will have to have their states changed? Connect the oscilloscope in such a manner that will verify the results. Draw the waveforms.

Logic Diagram

Waveforms

Input

Output

VIII. Draw a logic diagram of a circuit that will perform the functions of a foreshortened counter to six. It is a requirement that the stages must indicate the

number of pulses input for any number of pulses less than six.

IX. Manually step pulses into the circuit. Enter the state of each state in the table.

Input	Flip Flop 1	Flip Flop 2	Flip Flop 3

F. REPORT:

I. Perform the experiment as required in part E.

II. Discuss the ways that counters of various types can be used.

III. Why is it necessary to trigger successive states from the "0" side of the flip flop?

IV. Write an expression for the frequency divider that will give the number that must be added to the counter in terms of the desired frequency division and the next binary increment.

V. Construct a truth table for a five stage binary counter. When would the pulse to add numbers to the counter occur? If it is desired to divide the frequency by 21, what number would be added to the counter? What digits would be triggered? Draw a logic diagram that will perform this operation.

VI. Draw the logic diagram for a foreshortened counter that will count to 14. It is required that the stages indicate the number of pulse received for numbers less than 14.

G. REFERENCES:

I. Flores, Ivan. Computer Logic. Englewood, New Jersey: Prentice-Hall Inc., 1960

AIR FORCE INSTITUTE OF TECHNOLOGY

Department of Electrical Engineering

Laboratory Experiment No. EE-309-8

A. TITLE: Pulse Train Generators and Complementers

B. PURPOSE: To study the characteristics of complementers and to build logic circuits that will perform the complementing function and to study and build logic circuits that will perform the functions required of a pulse train generator.

C. DISCUSSION:

I. The two logic functions that are discussed in this experiment have no connection with each other and are in the same experiment coincidently. For this reason no attempt will be made to relate one part of the experiment with the other.

II. Whenever it is required to generate a fixed number of pulse to perform some logic function, a pulse train generator is used. A pulse train generator may be described as a device that will generate a preset number of pulses after receipt of a start signal. Upon completion of pulse generation, the pulse generator will initiate an end of pulse signal.

III. A pulse generator normally consists of a free running multivibrator, a pulse counter, and the necessary gating circuits that will perform the logic. There are two

types of pulse generators, synchronous and asynchronous. A synchronous pulse generator is a synchronous with the incoming start pulse. An asynchronous unit does not have this restriction. In many logic applications the asynchronous generator will suffice. (Ref 6:202)

IV. In many instances, it is inconvenient for the computer to perform arithmetic functions in the conventional manner. Instead the process of complementing is used. The theory behind complementing has been discussed previously in this course. Briefly complementing changes the process of subtraction to addition or vice versa.. The complement of a number is the difference between that number and the base of the complement. The most often used complements are the 9's complement and the 10's complement in the decimal based number system and the 1's and 2's complements in the binary number system.

V. To illustrate the complementing system, conside the decimal number 5. The 9's complement of 5 is 4. The 10's complement of 5 is 5.

or 9's complement + 1 = 10' s complement (1)

In the binary system, the complementing system becomes quite simple. For example, the 1's complement of 1 is 0 the 1's complement of 0 is one. Again the 2's complement of a number is the 1's complement plus 1.

VI. The complementing process can be expanded to binary codes. While the binary digit system is used, the complements can be expressed in the decimal system. The complements of Excess -3 coded decimal system is shown in Figure 1.

Decimal	XS-3	9's Complement
0	0011	1100
1	0100	1011
2	0101	1010
3	0110	1001
4	0111	1000
5	1000	0111
6	1001	0110
7	1010	0101
8	1011	0100
9	1100	0011

Figure 1

VII. Notice that to find the complement of a number in the XS-3 code, the only requirement is to exchange the ones and zeros. A code which exhibits this capability is called a self complementing code. (Ref 11:50)

D. EQUIPMENT:

I. Digital Bread Board
II. Oscilloscope
III. VTVM
IV. 4 Inverters
V. 3 2 Input "Or" Gates
VI. 1 4 Input "And" Gates
VII. 4 3 Input "And" Gates
VIII. 2 2 Input "Pulse And" Gates

E. PROCEDURE:

I. Draw the logic diagram for pulse train generator that, after receipt of a start signal, will generate a series

of ten pulses. Upon completion of the ten pulses, the pulse generator will generate an "end of pulse" signal. For the purpose of this problem, the start signal can be the DC reset pulse. Use the free running multivibrator set at IPPS for the pulse source.

II. Build the logic circuit in I above. Starting with the counter set at zero, determine the number of pulses that can be generated by the pulse generator. Record the necessary information to substantiate your design.

III.

NBCD Codes and NBCD Complement Codes

Decimal Digit	NBCD Code	NBCD Complement Code	Decimal Digit Complement
0	0000	1001	9
1	0001	1000	8
2	0010	0111	7
3	0011	0110	6
4	0100	0101	5
5	0101	0100	4
6	0110	0011	3
7	0111	0010	2
8	1000	0001	1
9	1001	0000	0

Figure 2

Using the 9's complements of the NBCD code shown in Figure 1 write the Boolean equations for each digit of the complement.

IV. Draw a logic diagram that will perform the complementing function of the Boolean equations given in part III.

Synthesize the circuit and take necessary data to substantiate your design.

V. Draw a table similar to that of Figure 2 for the NBCD code using the 10's complement instead of the 9's complement.

VI. Derive the Boolean equations for the complements digits.

VII. Draw a logic diagram that will perform the 10's complementing functions for the NBCD code. Synthesize the circuit and take necessary data to substantiate your circuit.

F. REPORT:

I. Perform the experiment as outlined in Part E.

II. How would you make an asynchronous pulse generator into a synchronous one? In general can synchronization be performed in one synch pulse on a free running multivibrator?

III. Discuss some of the ways that a pulse train generator can be used.

IV. Show that the 9's complement of the 5211 weighted decimal code is a self-complimenting coding system.

V. Develop the logic for an XS-3 complementer.

VI. Explain how the complement of a self complementing code system is readily available when the digits are stored in some two state device such as a flip flop.

G. REFERENCES:

I. Flores, Ivan. Computer Logic. Englewood, New Jersey: Prentice-Hall, Inc., 1960

II. Siegel, Paul. Understanding Digital Computers. New York: John Wiley And Sons Inc., 1961

AIR FORCE INSTITUTE OF TECHNOLOGY

Department of Electrical Engineering

Laboratory Experiment No. EE-309-9

A. TITLE: Arithmetic Logic

B. PURPOSE: To illustrate by design and implementation how functional units can be incorporated into complete arithmetic logic functions.

C. DISCUSSION:

I. Until the present, these experiments have been primarily concerned with the design and use of functional logic blocks. This experiment will be the first one in which functional blocks are combined to form some useful arithmetic logic that could be used in some actual digital computer.

II. The equipment listed in Part D includes three emitter followers. Little use has been made of these units in past experiments, but their use will be required in this one. Care must be taken to insure that the loading of logic devices does not occur. If in doubt, use an emitter follower. Most "And" and "Or" gates contain emitter follower within them and do not have to have an emitter follower to drive their output. Flip flops, shift registers, and other pulse generators do not have these integral emitter followers

and must be closely monitored to insure that they are not loaded excessively. In general if a pulse generating unit is driving more than three units, use an emitter follower. This is an emperical relationship and can be tested as you build the circuit.

III. Another factor that has not appeared to any great extent in previous experiments is the race condition. This condition is caused by changing of the state condition of some unit that is expected to drive some other logic device based on its previous or present state. The result can not necessarily be predicted in a logic diagram. The judicious use of delays can solve this problem. The exact nature of the race problem in this experiment is compounded by the slow speed (manual pulse and 1 pulse per second) that will be required in the experiment.

D. EQUIPMENT:

I. 2 Digital Bread Boards

II. Dual Trace Oscilloscope

III. VTVM

IV. 3 Emitter Followers

V. 4 2 Input Pulse "And" Gates

VI. 5 Inverters

VII. 3 2 Input "And" Gates

VIII. 1 3 Input "And" Gates

IX. 8 Shift Registers

X. 7 Flip Flops

XI. 7 Univibrators

XII. 1 2 Input "Or" Gates

XIII. 2 Half Adders (If half adders are not available, then additional logic units must be used to make a full adder.)

E. REPORT:

I. Draw the logic for an arithmetic unit that will perform serial addition subject to the following constraints.

a. The DC reset button can be used as a signal to add and to reset any binary counters used.

b. The system must respond to the manual pulse generator and to the clock generator set at 1 pulse per second.

c. The addend and augend must be parallel input into their respective registers.

d. The sum must appear in the addend accumulator at the end of the addition process.

e. The register will contain four bit storage elements.

f. At the end of the arithmetic process, there must be an indication of carry overflow or completion of operation.

g. Pulse input to the system must come from a single source.

II. Implement the logic diagram on the two bread boards. Connect the chassis grounds together. Check the voltage

levels on the two boards to insure that comparable voltages are the same.

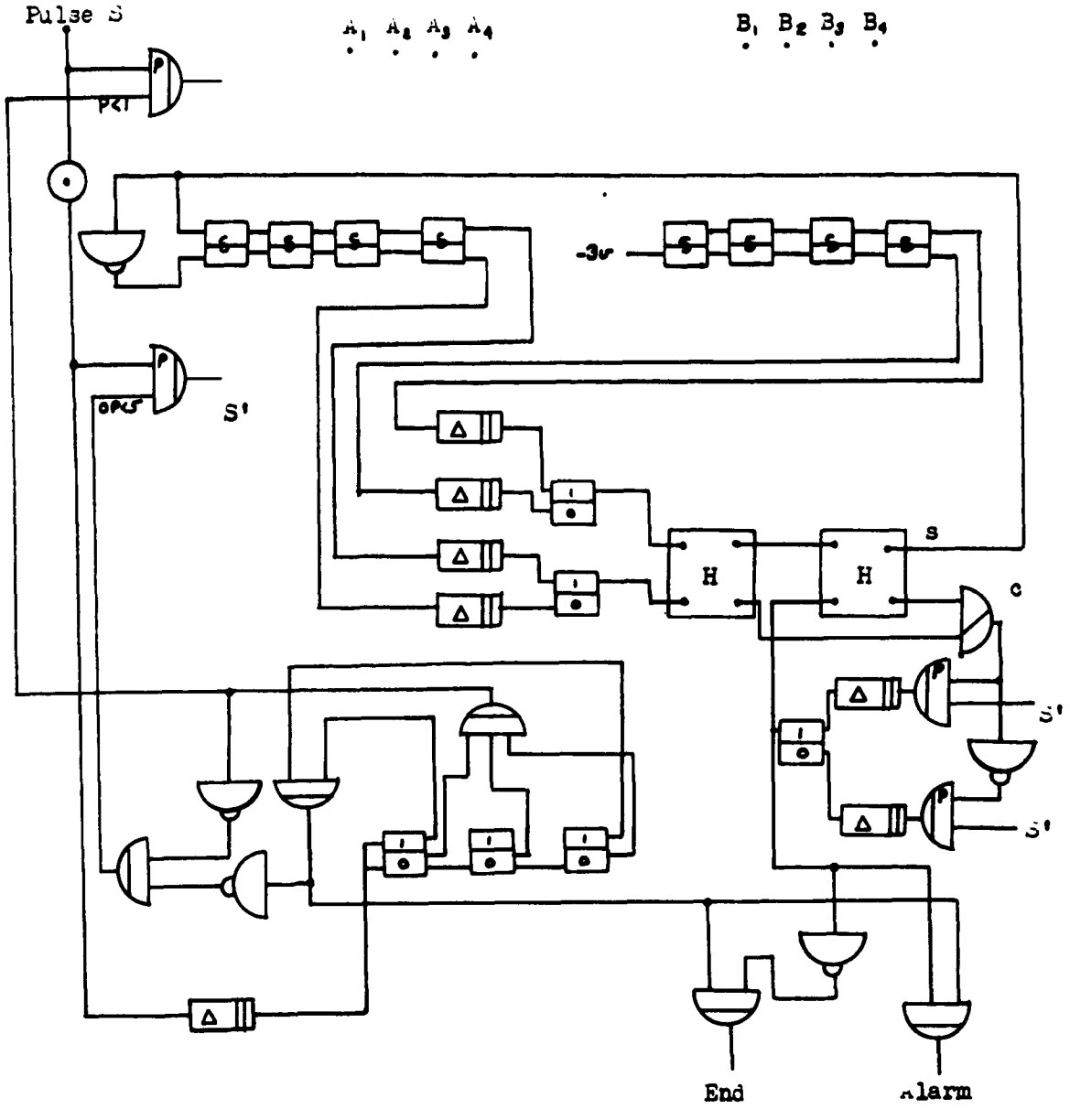
III. Put various numbers into the accumulators and check to see that the unit performs as it should. Troubleshoot the logic with the manual pulse generator. When the device is working, call your instructor to demonstrate its capability.

F. REFERENCES:

I. Flores, Ivan. Computer Logic Englewood, New Jersey: Prentice-Hall Inc., 1960

II. EECo Digital Circuit Modules Catalog T72. Advertising Catalog. Santa Ana, California: Engineering Electronics Company, n.d.

III. Siegal, Paul. Understanding Digital Computers. New York: John Wiley and Sons Inc. 1961.


Pulse S
A1 A2 A3 A4
B1 B2 B3 B4
P
PCT
C
-3v
OPCT
S'
H
H
S
C
S'
S'
End
Alarm

AIR FOR INSTITUTE OF TECHNOLOGY

Department of Electrical Engineering

Laboratory Experiment No. EE-309-10

A. TITLE: Logic Design

B. PURPOSE: To demonstrate the utilization of logic functions in design problems.

C. DISCUSSION:

I. All the logic circuits that have been discussed to date have had direct application in digital computers. This experiment will be concerned with these types of circuits but, in addition, will be concerned with circuits that can perform logic functions in other types of electronic equipment.

II. Your instructor will decide which of the logic functions will be implemented on the bread board and which will be merely drawn. Unless otherwise directed assume that the device must be controlled by the manual pulse generator.

D. EQUIPMENT: To be designated by the instructor.

E. REPORT: Obtain logic solutions to the problems below either by drawing logic diagrams or by implementation on the bread board. Specific instructions will be issued by the instructor.

I. Prepare logic that will take the representation of decimal digits 1 through 9, convert them into binary notation, and produce the nine's complement of the original decimal digit.

Both the input and the output should be represented by some predetermined light.

II. A certain pulse coded modulation signal consisting of eight bits is to be serially input into a device. Design a logic device that will produce a true signal if one of the following three conditions are met:

a. Four or more of the inputs are "1's".

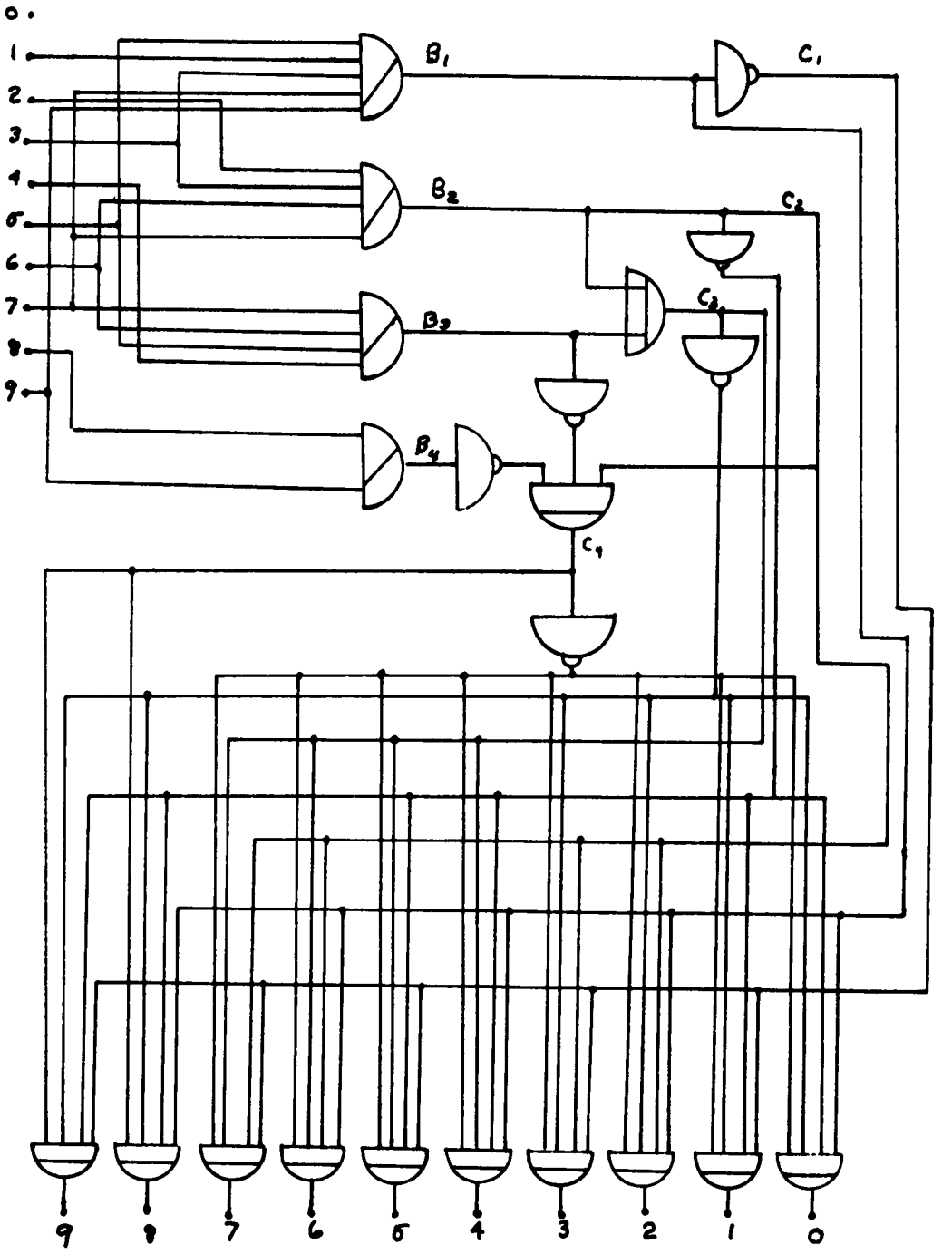
b. The eighth pulse is "1".

c. The second and the fifth pulse are "1's".

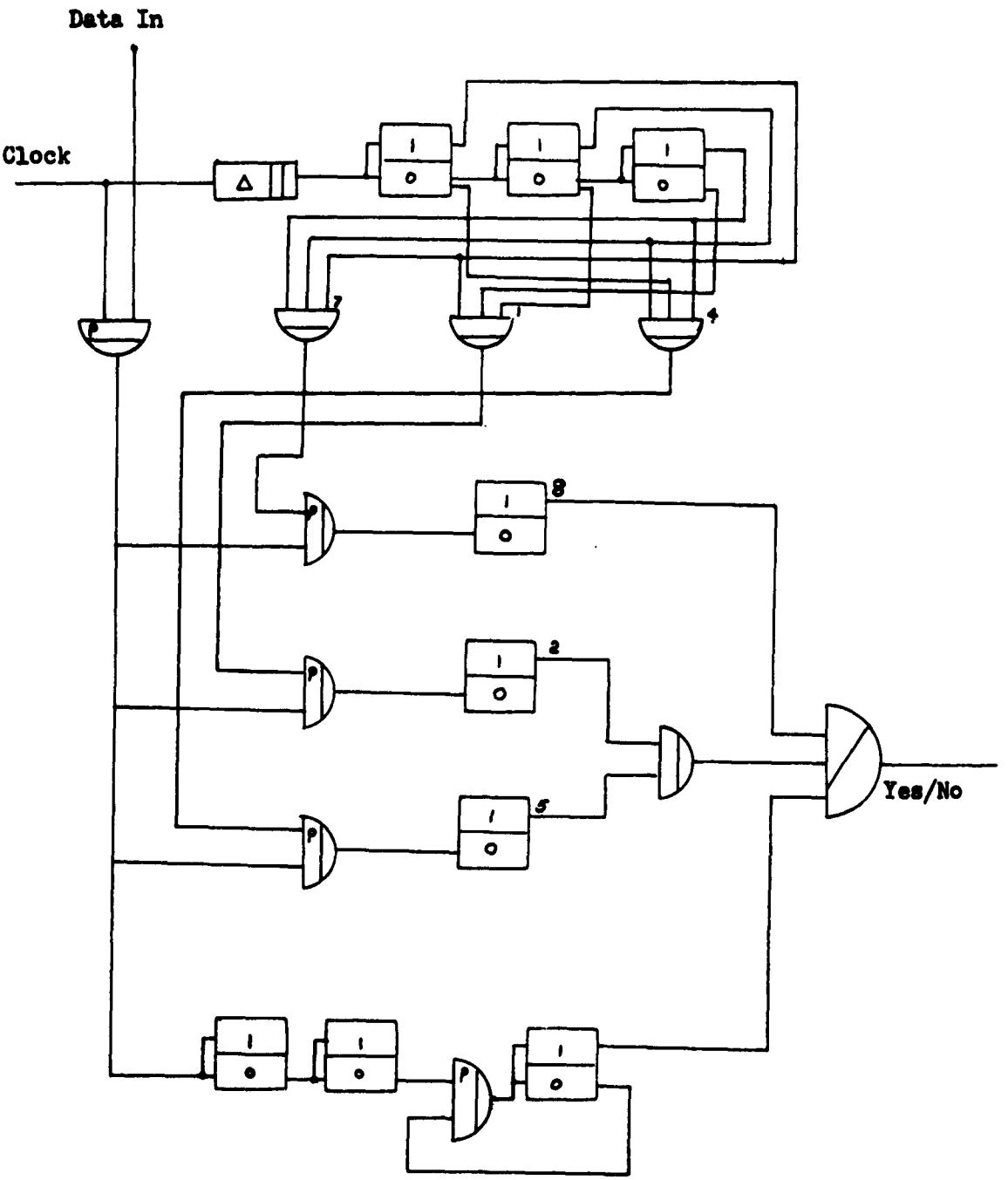
III. It is desired to modulate the output of the airborne transponder of the TACAN with a pulse code that will represent the aircraft's altitude. The code has been established to consist of five digits. The triggering signal of the TACAN consists of two pulses. Design a circuit that will generate the output required after receipt of the two trigger pulses from the TACAN output. Generate the trigger pulses with one manual pulse generator and the clock pulses with another manual pulse generator.

IV. A pulse code modulated signal consists of eight bits serially input to a shift register. Assume that the first pulse is some type of synch pulse that would normally synchronize the clock generator to the incoming pulse. The fourth and fifth pulse contain the binary code digits

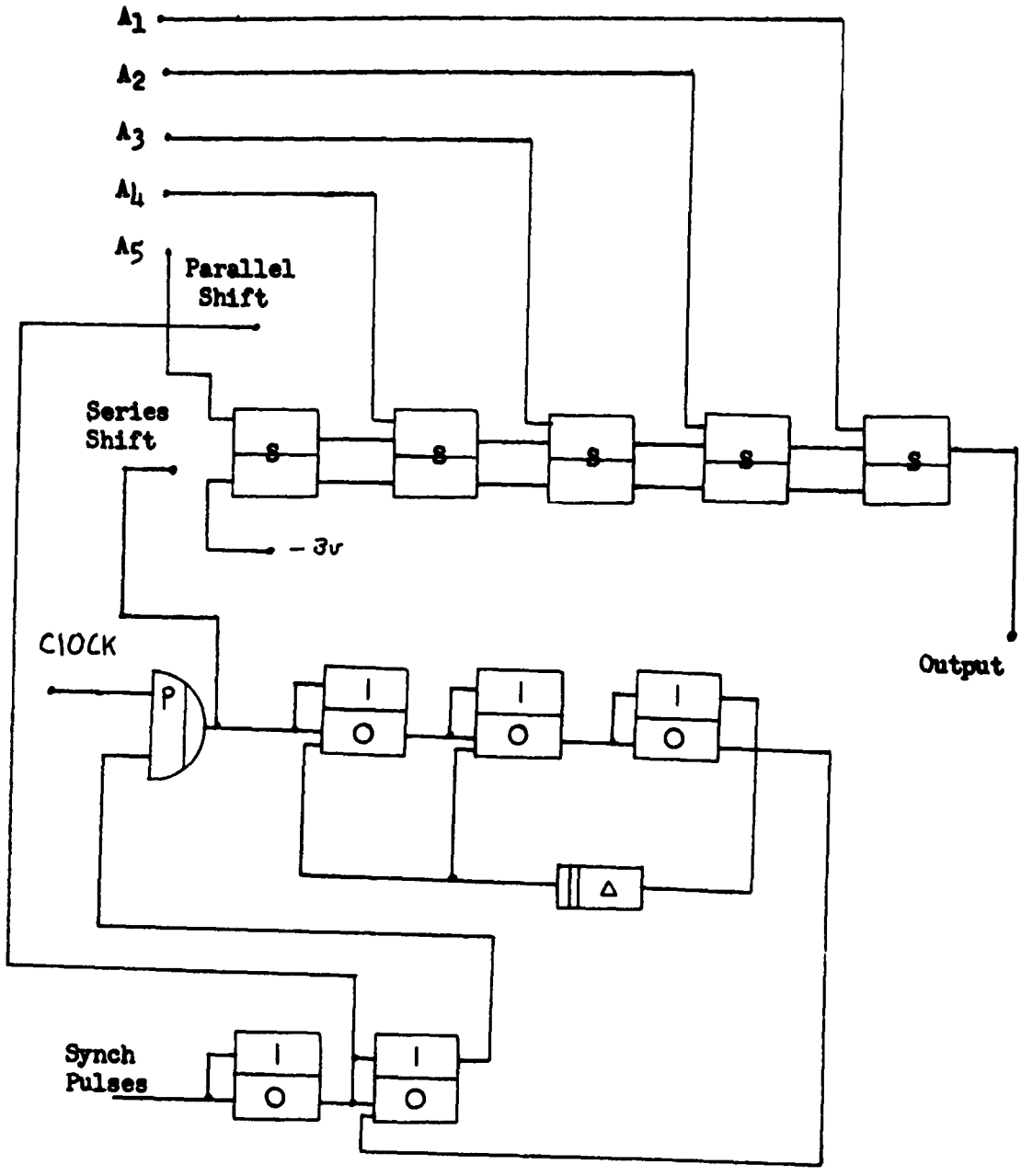
that are of interest. Design a logic circuit that will produce a decimal digit output based on the information contained in the fourth and fifth pulse. It is not necessary that the other digits be indicated. At the end of the signal the device must be capable of receiving new information.



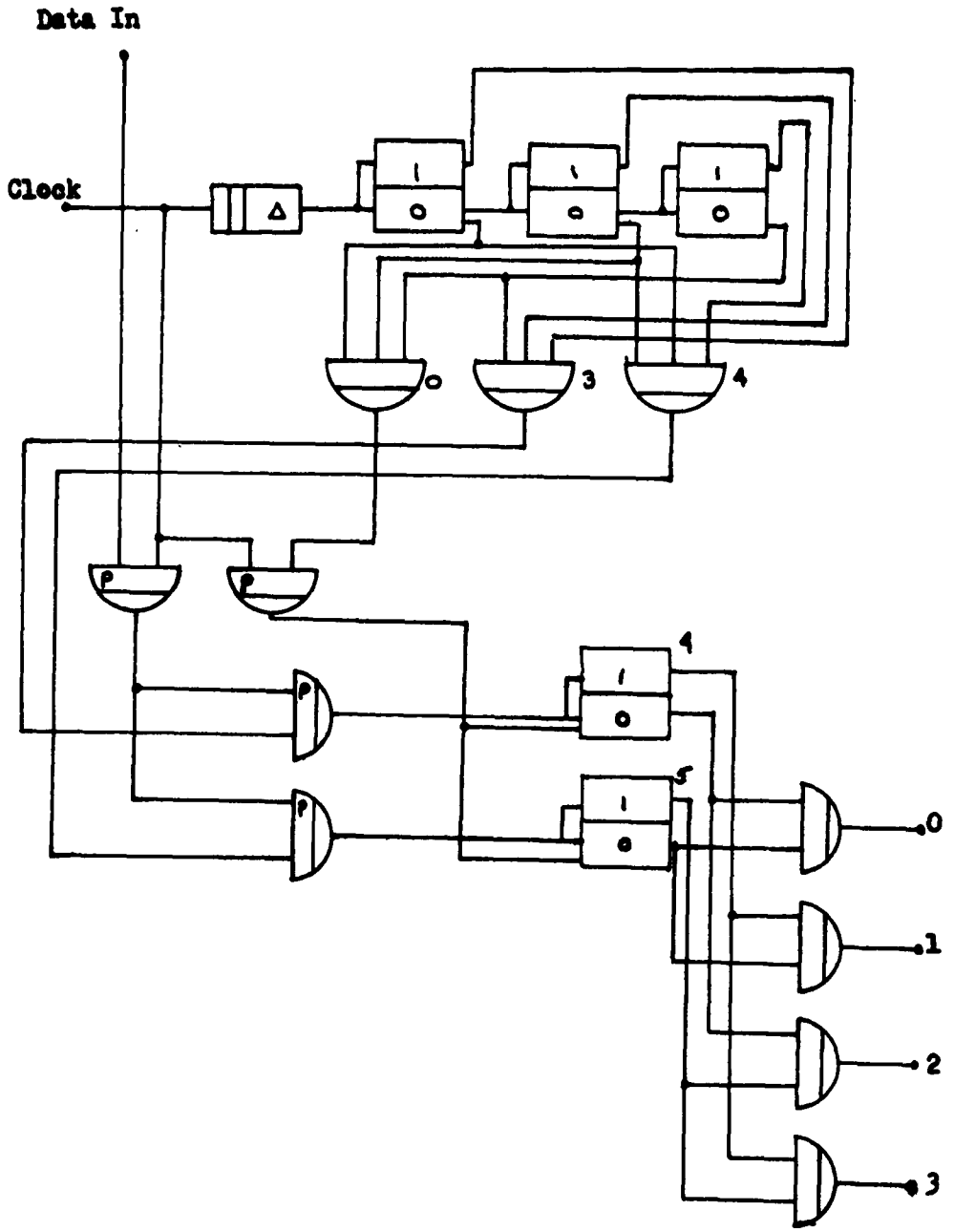
Experiment No. EE-309-10, Problem I, Solution



Experiment No. EE-309-10, Problem II, Solution



Experiment No. 309-10, Problem III, Solution



Experiment No. EE-309-10, Problem IV, Solution

Appendix B

Cost of Digital Bread Board

Unit	Type	No.	Cost/Unit $	Total Cost (1) $	Total Cost (2) $
T-113	Emitter Follower	2	21.35	42.70	85.40
T-448	2 Input Pulse "And"	4	48.90	195.60	391.20
T-136	Inverters	5	19.45	97.25	162.50
T-641	2 Input "And"	2	28.20	56.40	112.80
T-620	3 Input "And"	4	33.10	132.40	264.80
T-606	Shift Registers	8	53.05	424.40	699.20
T-101B	Flip Flop	10	34.80	348.00	677.50
T-166	Univibrator	7	38.40	268.80	431.20
T-642	2 Input "Or"	4	28.20	112.80	225.60
T-424A	Half Adder	2	34.95	69.90	139.80
				$1682.95	$3190.00

Module Cost (Ref 12:1-3)

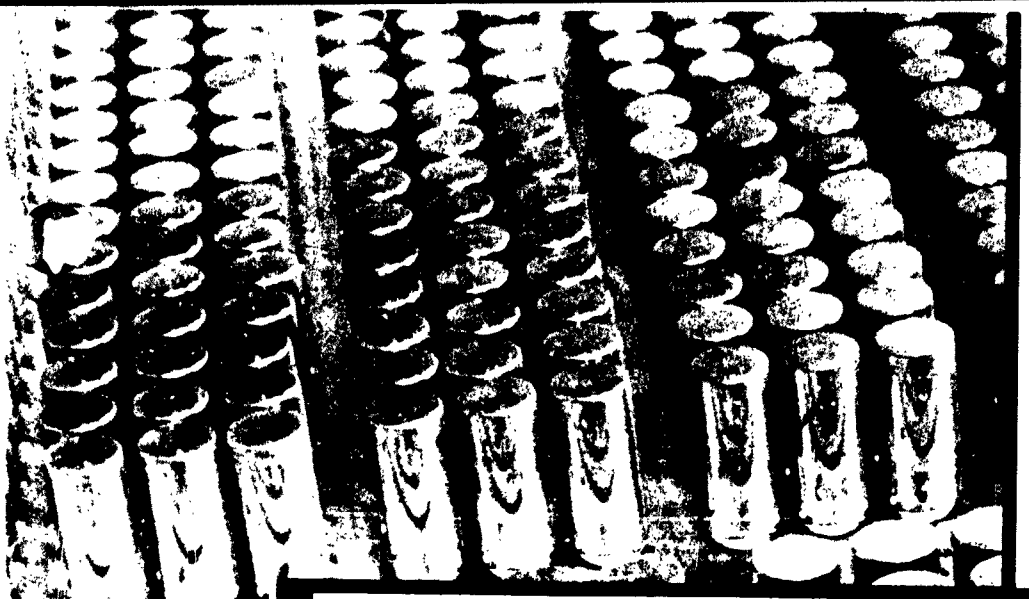
(1) This cost figure is based upon the minimum equipment that it would take to perform all experiments. It is based upon complete capability for simultaneous performance of experiments 2 through 8 by two groups and capability for one group to perform experiments 9 and 10. This figure does not include the Bread Board itself.

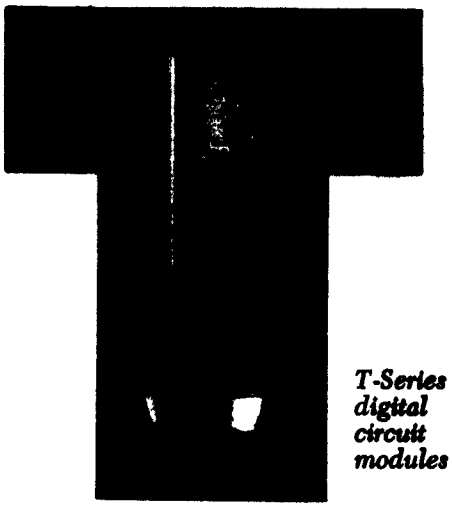
(2) This cost figure is based upon twice the capability of (1). Each Bread Board and its associated equipment costs $1422.00. To realize the capability in (1) would take two Bread Boards, so the total cost would be $4526.95. Total cost to realize (2) would be $8878.00.

Vita

George W. McKemie was born on 6 March 1935 in Baton Rouge, Louisiana, the second son of James B. McKemie and Elizabeth Wildes McKemie. He graduated from the United States Naval Academy at Annapolis, Maryland in June 1957 receiving the Degree of Bachelor of Science. He was commissioned Second Lieutenant, United States Air Force. His assignment prior to his coming to the Resident School of the Institute of Technology was with the Directorate of Materiel, Headquarters 86th Air Division (Defense) APO 12, U. S. Forces.

This thesis was typed by Mrs. Nellie M. Weaver.





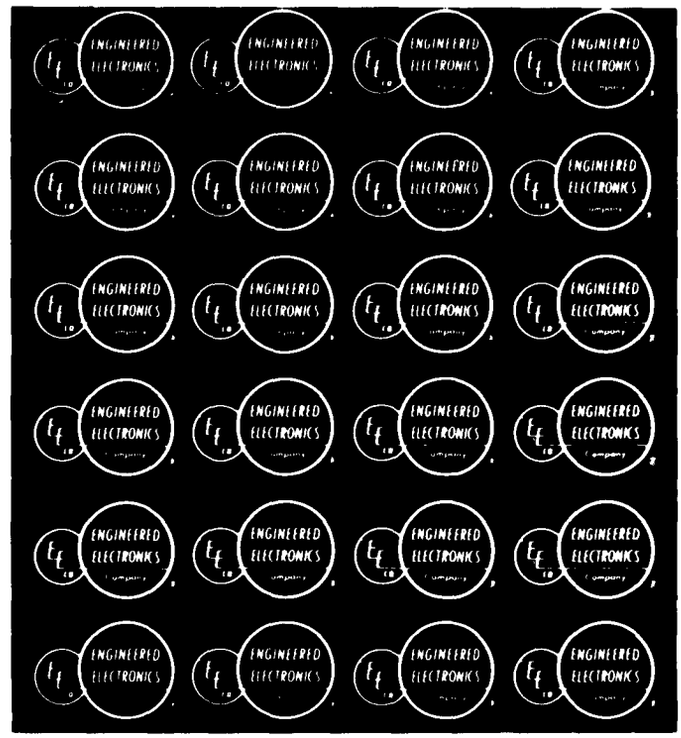
T-Series digital circuit modules

CT-Series digital circuit modules

EECo digital circuit modules catalog T72

PRESENTING ONE OF THE MOST COMPREHENSIVE, VERSATILE AND WIDELY PROVEN FAMILIES OF DIGITAL CIRCUIT MODULES EVER CATALOGED.

ENGINEERED ELECTRONICS Company



WARRANTY

Engineered Electronics Company hereby warrants standard catalog items of our manufacture to be free from defects. If **at any time** a module fails in normal service due to defective parts, workmanship or packaging, Engineered Electronics Company will repair or replace the module without charge, providing required parts are still available.

In addition, modules damaged by misuse, accident, neglect, or improper installation, will be repaired at cost.

ENGINEERED ELECTRONICS Company

ENGINEERED ELECTRONICS Company

1441 EAST CHESTNUT AVENUE SANTA ANA, CALIFORNIA
PHONE: 714-547-5651 • TWX: S ANA 5255 • CABLE: ENGELEX

EECo Catalog T-72

This catalog offers you fast access to information describing the most proven and widely used family of digital circuit modules available. Separate sections enable rapid location of data needed .These sections are:

INDEX, starting on the next page, shows the location of general family information, information for each circuit type and information on related equipment units.

GENERAL FAMILY INFORMATION, starting on page 7, covers specifications, construction, loading procedures, symbol definitions and other material that is common to all T- or CT- modules.

CIRCUIT DATA SECTION, begins on page 18. This section covers each module in detail. The units are grouped by circuit type and function and the functional groups are arranged in alphabetical sequence. For example, data on Emitter Followers are presented prior to data on Flip-Flops.

RELATED EQUIPMENT SECTION presents information on digital system breadboard equipment, power supplies, hardware, and panels and chassis. This section begins on page 65.

PRICES and ORDERING INFORMATION are provided on sheets in the back of this catalog.

SEE OUR SPECIFICATIONS IN VSMF THE MICROFILM CATALOG FILE

T series

CONTENTS OF THIS CATALOG

MATERIAL IN BACK OF CATALOG:

PRICES AND BUYING INFORMATION

T-SERIES MODULE NUMBER INDEX

EECo

SPECIALIZES IN DIGITAL CIRCUIT MODULES

There are many reasons that systems engineers, with an eye to critical deadlines and company profit, are today increased appreciation for EECo digital circuit modules.

EECo, Engineered Electronics Company, specializes in the production of efficient electronic "building blocks." This specialization assures EECo's customers of advanced circuit module techniques, a maximum variety of available module types, speedy off-the-shelf delivery, and reduced system checkout time. The mushrooming volume and diversity of electronic systems that use EECo modules is proof of EECo's ability to assure "pre-proven module performance with maximum reliability." In short, EECo's modules eliminate hours of circuit development, testing, correcting and re-testing from a system schedule, with appreciable savings to the system's total cost.

EECo FACILITIES

Strategically located on a 19-acre site in the heart of the new industrial area of Santa Ana, California, Engineered Electronics Company's modern plant and facilities are completely furnished with the latest equipment, including an integrated production line for welding under microscopes.

Also included is a bonded stockroom for Jan Mil parts. Present overall facilities clearance is to Confidential.

A complete evaluation of production runs is observed before any circuits are released. Quality-control testing is performed on a 100% basis, with quality control approved and under the cognizance of the U. S. Signal Corps.

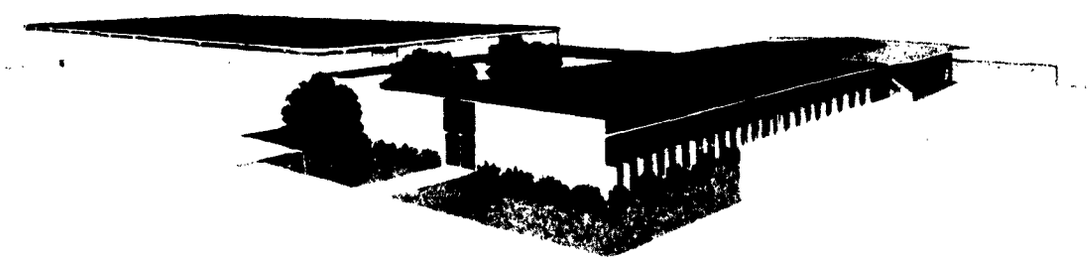
Accounting is under the audit of the U. S. Materiel Command.

EECo PERSONNEL

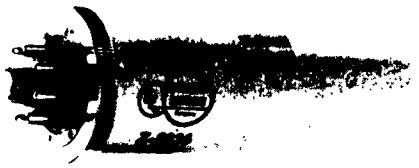
Engineered Electronics Company's entire top management are EE graduates. Twenty engineers are available at all times for circuit design and application counselling. In addition, we have 50 trained digital men in the field. All of our key personnel have secret clearance.

EECo PRODUCTS

EECo produces 8 cataloged circuit module families in addition to custom-produced modules, related breadboards, power supplies and hardware.

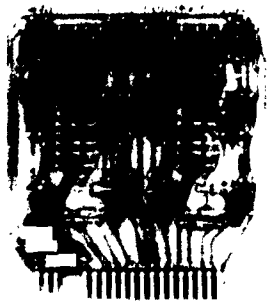


other EECo PRODUCTS



ELECTRON TUBE CIRCUIT PLUG-IN CONTAINER MODULES (Z-SERIES)

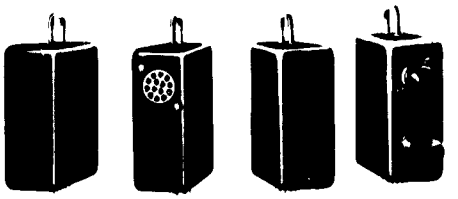
EECo's first "off-the-shelf" module series is still available in **Standard** units, for general applications, and **Ruggedized,** for more severe environmental conditions. Each Z-Series circuit contains one tube and is housed in a baked enamel container of die-cast aluminum. The 8 and 11 pin headers fit standard size sockets.



G-SERIES EXTENDED SERVICE DIGITAL CIRCUIT MODULES

The G-Series is a complete family of high quality, low-cost digital circuits on cards. Designed for either synchronous or non-synchronous applications, these units operate at frequencies up to 10 Mpps. For timing or nonsynchronous applications, G-Series units are used in conventional carry-trigger fashion without need for intervening amplifiers or special clocking techniques. For computing or synchronous applications, G-Series units are primarily used to implement logical expressions of the "And-to-Or" variety. Inherent flexibility of logic loading considerations permits rapid and uncomplicated system design.

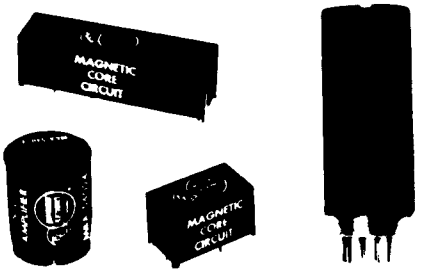
This family consists of four compatible sub-groups of circuits; sub-groups which operate at frequencies up to 10 Mpps, 5 Mpps, 500 Kpps, and 25 Kpps respectively. Each sub-group contains the necessary circuits to provide an attractive price advantage to the system designer . . . it is not necessary to pay for higher frequency capability than is necessary for each system or portion of a system.



TRANSISTOR DECADE COUNTERS (N-SERIES)

N-Series Plug-In Decade Counters feature high-operating speed, simple power requirements, and three types of readout. The three types of readout are: (1) a vertical display using ten incandescent lamps, (2) an in-line display using a NIXIE Tube, and (3) a remote projection-type display. All counters in the N-Series family are completely compatible with the T-Series Digital Plug-In Circuits.

These Decade Counters are also available in circuit board form.



MAGNETIC CORE-TRANSISTOR ENCAPSULATED MODULES (M-SERIES)

M-Series Magnetic Core-Transistor Circuits include a wide selection of shift-register elements, pulse-gates, and core-drivers. Twenty units of the family are intended for shift-register application and are packaged in containers identical to the T-Series containers. These twenty units are electrically compatible with the T-Series units and thus provide additional choice in the design of digital systems and equipment. Remaining units of the M-Series family are for general application and are available in a choice of two encapsulated packages; a cylindrical package which plugs into miniature-relay-type sockets or a rectangular package for installation on circuit cards.

MINISIG® INDICATORS (R-SERIES)

R-Series Minisig Indicators are sensitive indicator devices used to indicate the state of a flip-flop or storage element. Most Minisig indicators incorporate a driver circuit in order to give on-off indications where the signal excursion or power output is too small for direct operation of neon or incandescent lamps, and can, therefore, be used effectively in systems designed for small signal excursions.

These indicators are available in a variety of models including neon-type, filament-type, high-temperature-type, and thyratron-type units. Most models have adjustable operating characteristics controlled by external bias voltage to accommodate a wide range of input signal conditions.

TRANSISTOR UNIVERSAL NOR WELDED MODULES (U SERIES)

The universality of the U-Series is illustrated by the fact that only four basic module types (a dual NOR circuit, a dual Power Driver, a Converter, and a dual Pulse Gate) are needed to form a complete product line for any given frequency range. The full economy of this series is realized in systems using extensive amounts of logic.

U-Series modules can also form flip-flops, multivibrators, one-shots, and other active circuits in simple two-module assemblies. These modules are available in a choice of soldered or welded configurations and are available in two encapsulated shapes . . . rectangular for dense circuit-card assemblies, and cylindrical for use with breadboard kits or relay type sockets in conventional chassis applications.

MINIWELD® SYSTEM CIRCUITS (K and L SERIES)

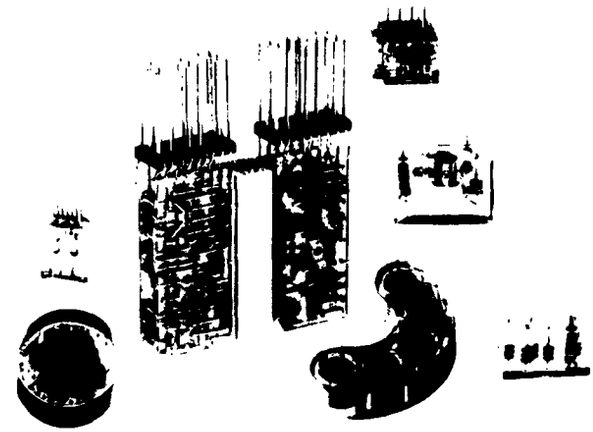
Highly developed welding and matrix methods pack up to 40 components into one L-Series module which occupies less than 2.5 cubic inches. There are 152 compatible modules in the L-Series.

K-Series units are economical breadboard versions of the more-expensive welded L-Series modules. A careful analysis of various systems requirements provided EECo with the ability to generate only 14 types of these K-Series units which enable economical breadboard simulation of all 152 L-Series modules. Use of K-Series units permits breadboarding a complete system or any portion of a system without expensive "prototype system" expense.

SPECIAL AND CUSTOM CIRCUITS

We invite quotation requests to produce special units tailored to your specific needs. Because of our experience in package design and assembly methods, we can produce these specials at a cost favorably comparable to the cost of producing an equal number of standard items. Prices on your special circuits can be estimated within 15% to 25% by comparing your circuits to similar circuits in the EECo catalog. When quotations are requested, or when orders are placed on an "advise-price" basis, the following information is required:

1. Circuit schematic.
2. Bills of Materials with:
   - Transistor, tube, or diode types.
   - Resistor values, tolerances, wattages, and temperature coefficient.
   - Capacitor values, tolerances, voltages, and temperature coefficient.



PACKAGING OF CUSTOM WELDED CIRCUITS

EECo has complete facilities for production packaging of welded circuits. We maintain a staff of packaging engineers, a metallographic lab and a plastic chemistry lab to assist you in custom packaging of your circuits.

T general family informatio

This section covers the general features, construction and specifications common to all T or CT Series modules. Of particular interest is the new loading information beginning on page 12.

Typical T-Series plug-in package, actual size.

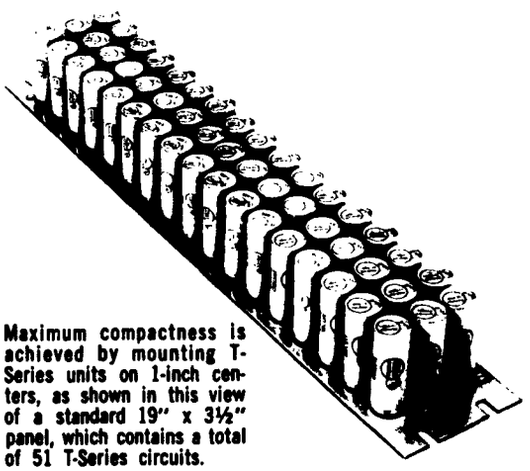
Typical T-Series construction details, actual size. (Patent #2986675)

T-SERIES transistor circuit plug-in digital modules

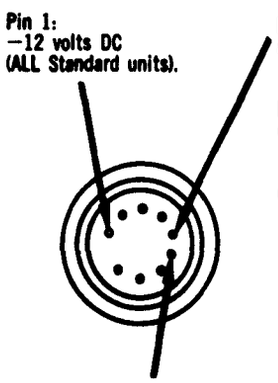
The T-Series is a *family* of transistorized digital circuits for service in compact systems and equipment.

Featured in the T-Series are:

1. *Compatible, standardized signal levels.*
2. *Consistently conservative electrical specifications.*
3. *Standard package outline.*
4. *Simple power requirements.*
5. *Electrical compatibility with N-Series Decades, R-Series Minisig® indicators, and M-Series Magnetic Core-Transistor Encapsulated Modules.*
6. *Choice of repairable modules, encapsulated modules for industry, and encapsulated modules for military applications.*



Maximum compactness is achieved by mounting T-Series units on 1-inch centers, as shown in this view of a standard 19" x 3½" panel, which contains a total of 51 T-Series circuits.



In general, circuit design is based on *saturated* operation of the transistors involved, except where fully reliable performance can be achieved using *unsaturated* operation. Each circuit design is based on derated specifications for the components used; and the resulting circuit specifications are then further derated to give reserve reliability. (For example, the guaranteed operating frequency range of a typical T-Series circuit may be derated by as much as 50%.)

The usual *operating* temperature range for T-Series circuits is −45°C to +65°C, with variations as noted on the individual specification sheets. Many circuits will operate over a range of −54°C to +71°C. *Storage* temperature range is −55°C to +75°C. The specifications for each circuit apply throughout the operating temperature range, and are guaranteed *minimum* specifications. As a result, if the ambient temperature is stabilized, the frequency range, loading capability, etc., of the circuits involved will generally be improved.

T-Circuits are also available in potted (TE) and circuit-card (CT) forms as well as with military components (TM) or military-equivalent components (TA). Delivery time for these special configurations is determined, to a great degree, by accessibility of parts. However, EECo maintains a bonded stockroom of MIL parts and long-delivery-time problems are rare. Prices for TM, TA, and TE units must be quoted by the factory.

POWER CONNECTIONS

Power connections are standardized throughout the T-Series to the greatest degree consistent with the most effective use of the number of pins available. For standard catalog circuits, the following uniform pin connections are used to simplify buss wiring of sockets:

1. In all cases, **without exception:**
   Pin 1 = −12 volts DC
2. In most cases, **with typical exceptions** as noted:
   Pin 6 = 12 volt common
   EXCEPTIONS:
   PNP emitter followers and DC Logic units require both a +12 volt DC and a −12 volt DC supply in contrast to other units, which require −12 volts DC only. On these units:
   Pin 6 = +12 volts DC
   (Examples: PNP emitter followers T-111, T-112, and T-113; DC Logic units T-404, T-405, T-406, and T-407.)
3. In some cases:
   Pin 5 = +12 volts DC
   (Example: Pulse "And" Gate T-410A.)

T-SERIES HARDWARE

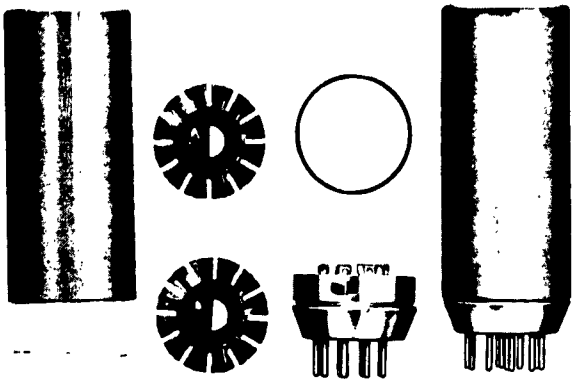
Blank T-Series containers, as well as accessory hardware for companion equipment, are available in limited quantities for prototype development or for "one-of-a-kind" circuits. A complete listing of available hardware may be found in the price list.

PART NUMBERING SYSTEM

T-Series part numbers are coded according to number of connector pins and circuit function. All catalog units have 3-digit part numbers; 4- and 5-digit numbers are used only for special and custom units. The numbering system for T-Series units is as follows:

Number	Socket	Circuit Type	Max Oper Freq
T-100	9-pin	Active	250 Kc
T-300	9-pin	Active & Logic	1 Mc
T-400	9-pin	Logic	250 Kc
T-600	13-pin	Active & Logic	250 Kc
T-800	13-pin	Active & Logic	1 Mc
T-900	——	Hardware	——

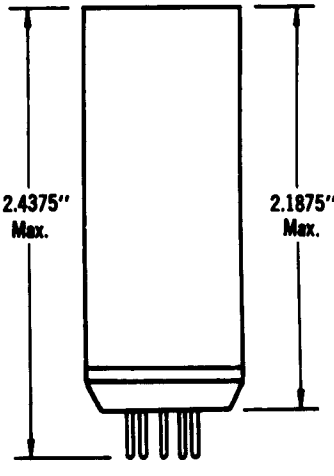
T-SERIES HARDWARE



T-906 T-Series container parts include 13-pin header and two discs. Also available with three discs as T-908. (Patent 2986675)

T-904 T-Series container is identical with T-906 (shown above), but is supplied with 9-pin header. (Patent 2986675)

T-937 Socket, 14-pin, with pin 10 plugged for keyway orientation. Mates with T-906, T-908, or any 13-pin T-Series unit. These sockets are supplied with the appropriate T-Series units at no charge. T-910, 9-pin sockets are not supplied with 9-pin T-Series units because these are standard tube sockets and usually already carried in customers' shelf stocks.



End view of typical 9-pin T-Series unit. Mates with standard 9-pin miniature noval socket. Standard miniature tube hold down hardware may be used.

End view of typical 13-pin T-Series unit. Mates with standard 14-pin miniature socket with pin 10 blanked for keyway orientation (EECo Part No. T-937). Standard miniature tube hold down hardware may be used.

OUTLINE DRAWINGS

T-SERIES DESIGN PHILOSOPHY

EECo T-Series circuits are designed to accommodate "worst case" situations where each component can deviate to the limit of its tolerance in the "worst" direction and at extremes of temperature. The circuits are tested at the temperature extremes both in breadboard and final evaluation states to assure that all specifications are met.

The use of ±12 volts was a matter of decision and compromise. These power levels were selected because of the following advantages:

A good safety factor for the breakdown voltages of the transistors used.

A good compromise between high voltage and good signal level, resulting in a good signal-to-noise ratio.

The low end of aircraft 28 volt supply tolerance is 24 volts (which is easily separable to ±12 volts). Our units will work on ±14 volts with only slight changes in specifications.

The units can work from standard automobile or marine battery voltages.

"True" and "false" levels of −3VDC and −11VDC respectively were selected in order to keep the number of power supply voltages required to a minimum. With these levels, it was possible to design many circuits requiring only one power supply. If one level were to be clamped at 0 volts, more elaborate circuitry would have been necessary and another design philosophy — circuit simplicity — would have been violated.

As with most engineering decisions, there are pros and cons regarding use of saturated vs. unsaturated techniques in the design of our units. First, the major disadvantage of saturated operation is that charge (minority carriers) is stored in the base region of the transistor during saturation and these minority carriers must be removed before the transistor can come out of saturation. This takes time and makes saturated operation more difficult at the higher frequencies. The stored base charge rating of the transistor then becomes a critical parameter. However, advantages of saturated operation are:

Simplicity of circuit design.

Well defined voltage levels.

Fewer parts required than in non-saturating circuits.

Lower transistor dissipation when conducting.

Immunity to short stray voltage signals.

Less dependance on transistor parameters.

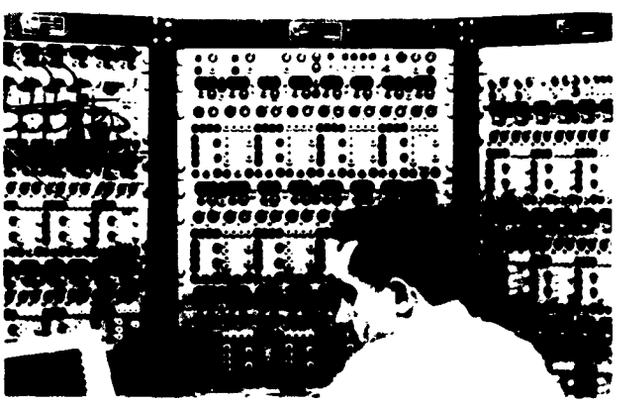
For these reasons, most of our T-Series circuits are designed for saturated operation.

DIGITAL SYSTEMS BREADBOARD KIT

The EECo Breadboard Kit for use with plug-in circuits is a powerful systems-design tool for the engineer, and also is valuable as a training and educational aid. The breadboard panels have the necessary permanent wiring to accommodate any regular circuit and all other circuit interconnections are made by patch cords or plugs. Therefore, no soldering is needed, and experimental arrangements of T-Series units can be quickly set up, changed, or taken down without waste of time or materials.

The breadboarding system is designed around plastic circuit cards with circuit symbols showing input and output connections, power connections, part number, application notes, etc. These cards fit on the panel below sockets for the plug-in units, and match a pattern of banana jacks that are permanently wired to pins on the sockets. Holes in the circuit cards expose the appropriate socket pin connections. Power connections are made by shorting plugs, which also align the cards with the jack pattern and hold the cards in place. Signal connections are made by patching card-to-card in the circuit line-up being tried.

All T-Series units **with pin 1 used for −12 volts,** whether 9-pin, 13-pin, or special units, can be used on the breadboard panels.



LOANER POLICY

We are prepared to loan you, without obligation, a reasonable quantity of EECo plug-in units for a 30-day trial period.

In order to obtain merchandise on a 30-day loan, send us a purchase order for the required units with a notation on the purchase order that the units are being ordered on a 30-day loan basis. The merchandise will be shipped to you with our regular invoice; terms are net 30 days from date of invoice. When you return the material, please return one copy of our invoice with the material and your account will be credited. You will be charged only for repair of damage to the units caused by misuse, neglect, accident, or improper installation or application. (See our Warranty in the Price List section of this catalog.)

EECo CT-Series Digital Circuit Card Modules

EECo's CT-Series is a fully compatible family of germanium transistor digital circuit modules on epoxy circuit cards. Every CT circuit is doubly-proved. First, CT circuits are basically card mounted versions of EECo's famous, time-proved, container-enclosed T-Series circuits. Second, the specific circuits selected for the CT family have proved most efficient in T-Series applications. Specifications for CT modules are identical to the corresponding T-Series modules (See Equivalent List below) except the CT-Series Operating Temperature range is −20°C to +50°C, and the power requirements are a multiple of the number of circuits per card.

CT circuits are wired with 2-mil copper bonded to etched 4-1/2" x 5" x 1/16" epoxy cards. Standard connectors are tin-plated, with optional Varicon, gold-plated, and rhodium-plated connectors available if specified. Card files, guides, connectors, and other hardware available for this series are described under "Hardware."

CT NUMBERING SYSTEM

A CT circuit number is the same as the number of its T-Series equivalent. A figure is appended to this figure to indicate the number of "T" circuits on the CT-card. No additional letter is needed for cards with standard tin-plated connectors. A letter is added to indicate other connectors:

V=Varicon
G=Gold-plated
R=Rhodium-plated

Example:

original T-Series circuit
number of "T" circuits on card
type connectors

CT-101B-3V

CT-Series modules can be used with card files, card drawers, and other hardware suitable for the 4-1/2" x 5" x 1/16" cards. The hardware shown in the hardware section of this catalog is specifically recommended and can be ordered from EECo, using the "H" part numbers listed in the Price List section of this catalog. For the convenience of companies supplied directly by the manufacturer, the manufacturers' part numbers are shown (in parenthesis).

CT #	T-SERIES EQUIVALENTS
CT-101B-3	Three T-101B RST Flip-Flops
CT-102A-4	Four T-102A T Flip-Flops
CT-104-2	Two T-104 Multivibrators
CT-109-4	Four T-109 Reset Generators
CT-106-4	Four T-106 Squaring Amplifiers
CT-111-9	Nine T-111 PNP Emitter Followers
CT-114-9	Nine T-114 NPN Emitter Followers
CT-134-4	Four T-134 Relay and Indicator Drivers
CT-136-4	Four T-136 Inverters
CT-162-4	Four T-162 RS Flip-Flops
CT-163-3	Three T-163 DC Drivers
CT-165-4	Four T-165 Capacity Drivers
CT-166-4	Four T-166 One-Shot Multivibrators
CT-302-2	Two T-302 Capacity Drivers
CT-304-4	Four T-304 Complementary Emitter Followers
CT-306-2	Two T-306 Squaring Amplifiers
CT-307-4	Four T-307 Dual Complementary Emitter Followers
CT-421A-4	Four T-421A Exclusive-OR Gates
CT-430-4	Four T-430 Pulse Mixer Amplifiers
CT-448-2	Two T-448 Dual Pulse "And" Gates
CT-605-3	Three T-605 Shift Register Flip-Flops
CT-606-2	Two T-606 Shift Register Flip-Flops
CT-641-2	Two T-641 Dual DCTL "And" Gates
CT-642-2	Two T-642 Dual DCTL "Or" Gates
CT-645-2	Two T-645 DCTL "NOR" Gates
CT-650-2	Two T-650 Dual DCTL "And" Gates
CT-651-2	Two T-651 Dual DCTL "Or" Gates
CT-801-2	Two T-801 Flip-Flops
CT-802-2	Two T-802 Dual DCTL "And" Gates
CT-805-2	Two T-805 Dual "Exclusive-OR" Gates

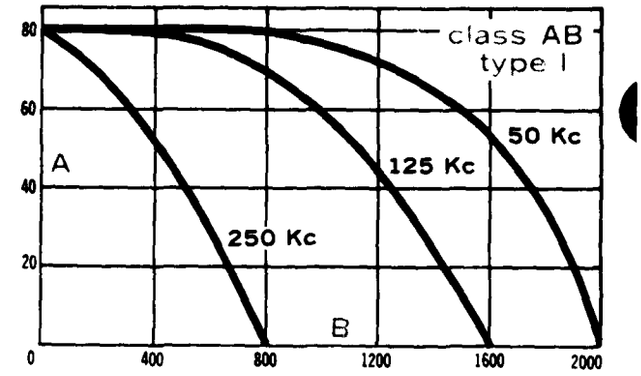
LOADING INFORMATION

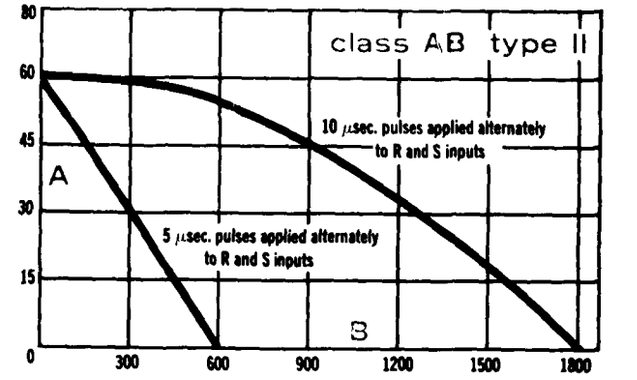
Individual unit specifications list input load characteristics in terms of arbitrary units, and output drive capabilities in terms of reference curves. This section of the catalog contains these reference curves, an explanation of how to use them, and other significant information to assist the digital system designer. An important point to remember is that these curves were generated for various typical operating frequencies with units operating at room temperature and with system power at 12 volts. Some derating is necessary at extremes of temperature or if system power varies over the specified tolerance.

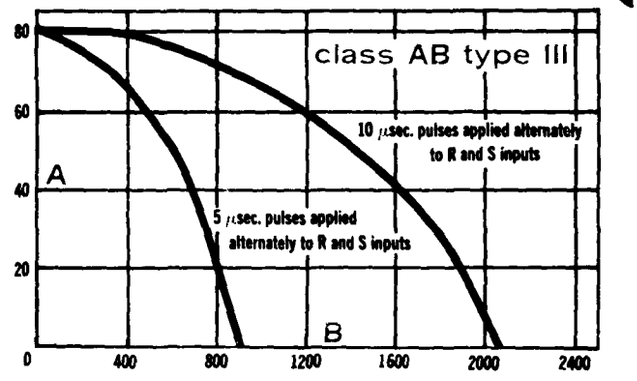
All T-Series circuits, depending on type of output, have one of three types of drive characteristic; AB, CD, or EF. All units with PNP-common-emitter output stages exhibit AB drive characteristics; units with PNP-emitter-follower output stages have CD drive characteristics; and, T-Series units with NPN-emitter-follower output stages have EF output drive characteristics.

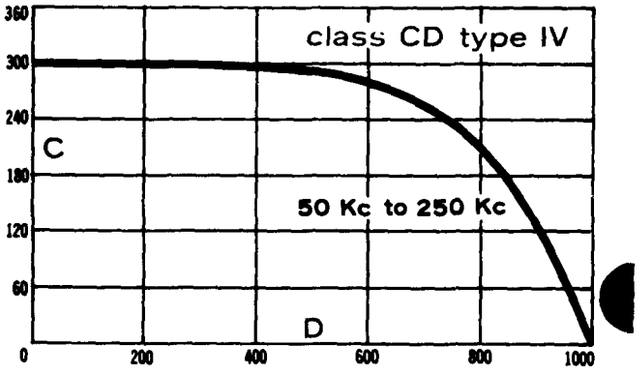
Similarly, T-Series units have three sets of input load characteristics; A & B, C & D, and E & F. The input characteristic to be used in a given system application depends on the drive characteristic class of the circuit used as a driver. AB drivers will "see" A and B input characteristics; CD drivers will "see" C and D, etc. If a given type AB driver is to drive a variety of other circuits, then all the A input characteristics of the driven circuits should be added algebraically and all the B characteristics of the driven circuits should, similarly, be added algebraically. The total A's and B's are then located on the reference curve for the driver and, if the AB coordinates are within the maximum shown on the chart, the driver will drive the circuits.

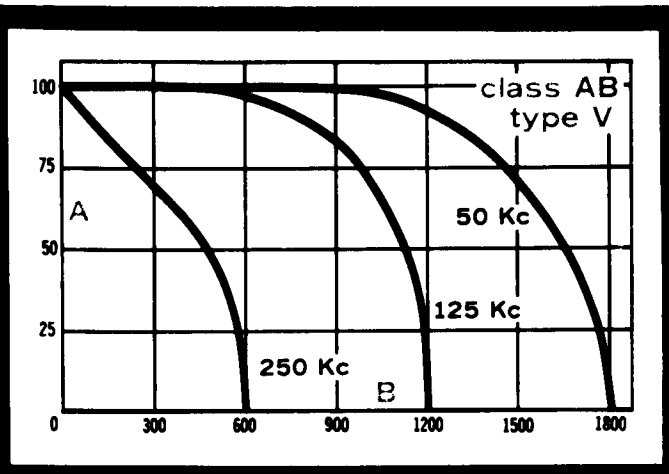
For example, consider the case where a T-101B flip-flop being triggered at 250Kc is to trigger four other T-101B flip-flops. Since the T-101B, in a T mode of operation, is an AB type I driver, the A and B input characteristics of the driven circuits must be summed. A=10 and B=100 for a single T-101B flip-flop, hence four T-101B's represent a total A load of 40 **and** a total B load of 400. Application of these AB values as coordinates to the drive characteristic curve AB Type I reveals that a T-101B being triggered at 250Kc can reliably trigger four other T-101B's.

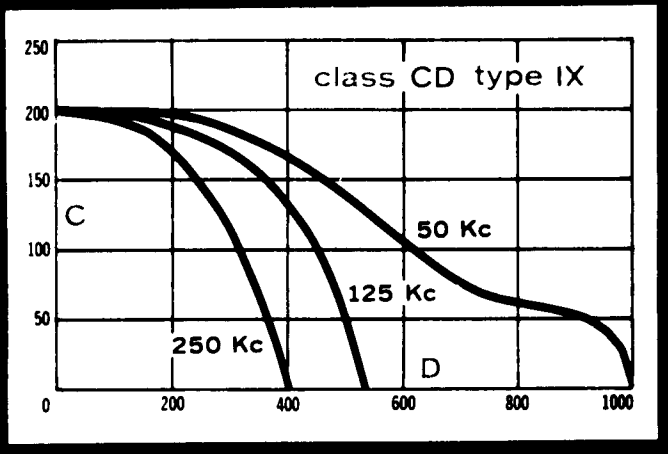


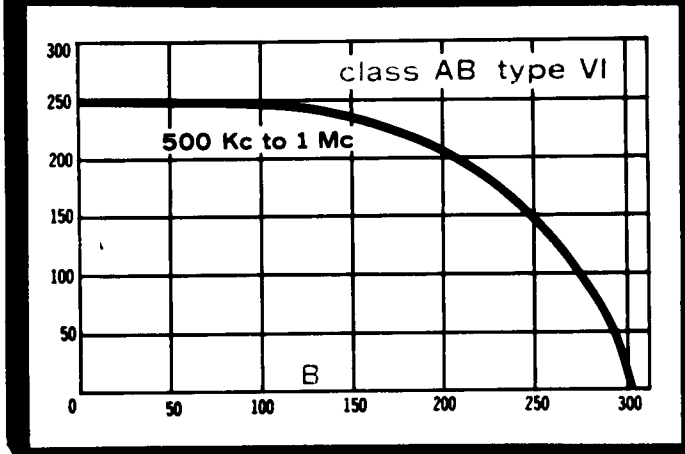


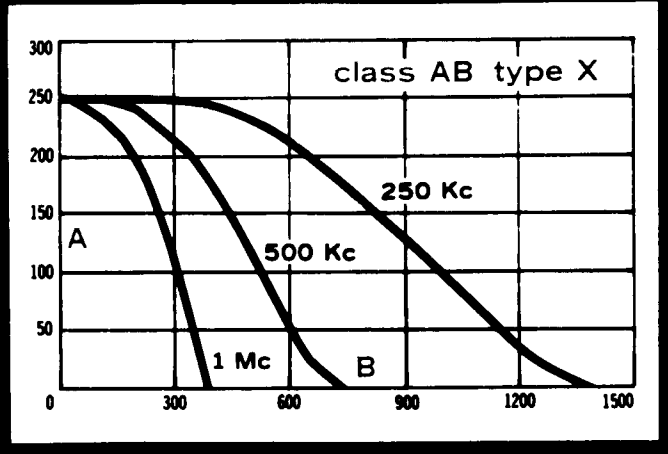


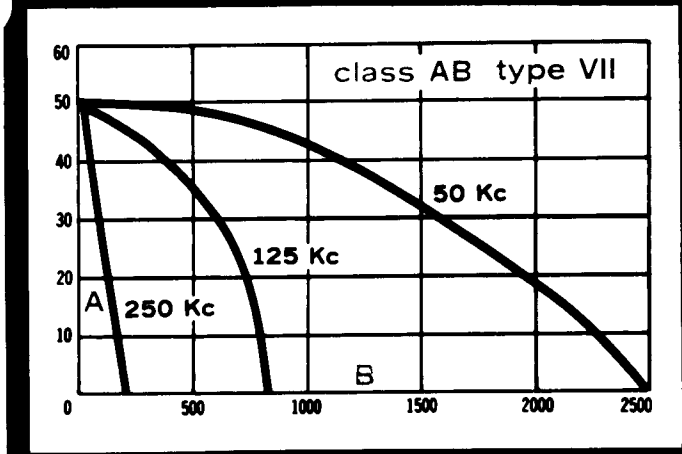


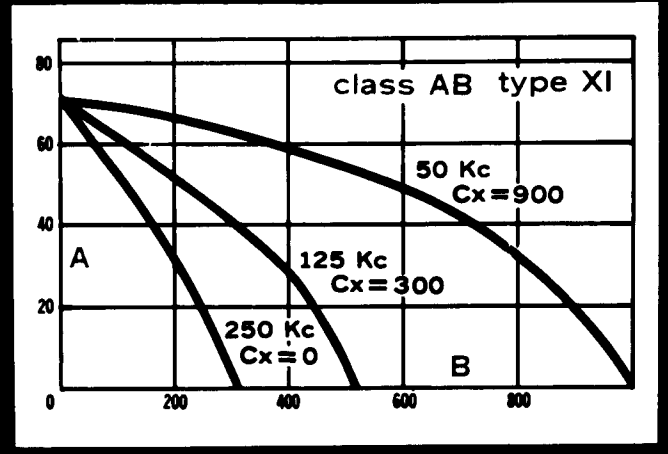

class AB
type V
A
50 Kc
125 Kc
250 Kc
B
100
75
50
25
0
300
600
900
1200
1500
1800

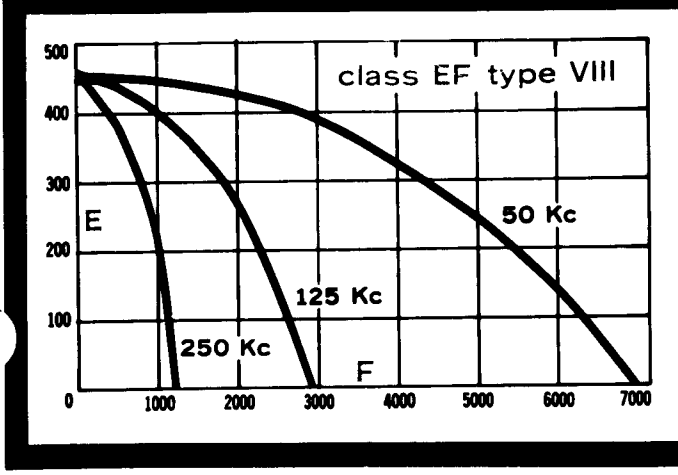

class CD type IX
C
50 Kc
125 Kc
250 Kc
D
250
200
150
100
50
0
200
400
600
800
1000

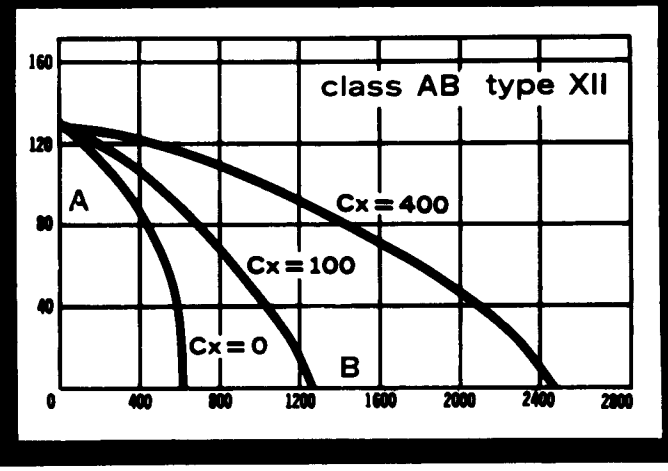

class AB type VI
500 Kc to 1 Mc
B
300
250
200
150
100
50
0
50
100
150
200
250
300

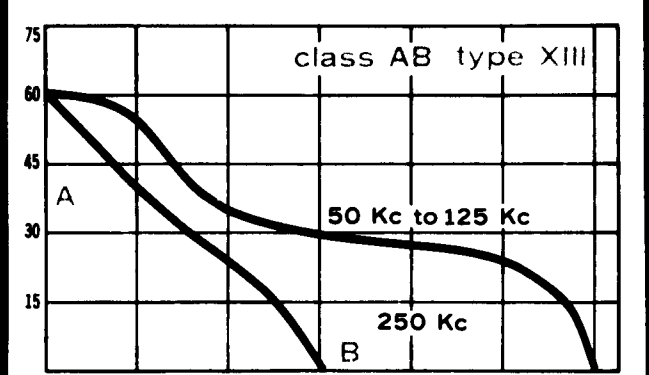

class AB type X
250 Kc
A
500 Kc
1 Mc
B
300
250
200
150
100
50
0
300
600
900
1200
1500

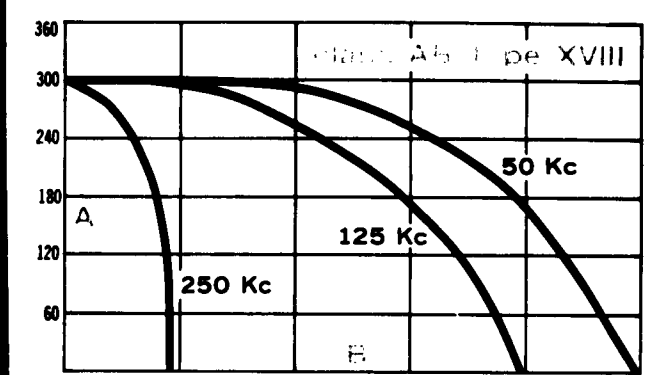

class AB type VII
50 Kc
125 Kc
A
250 Kc
B
60
50
40
30
20
10
0
500
1000
1500
2000
2500

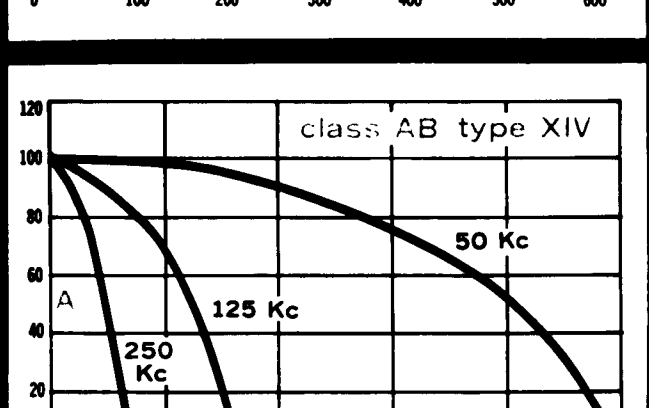

class AB type XI
50 Kc
Cx=900
A
125 Kc
Cx=300
250 Kc
Cx=0
B
80
60
40
20
0
200
400
600
800

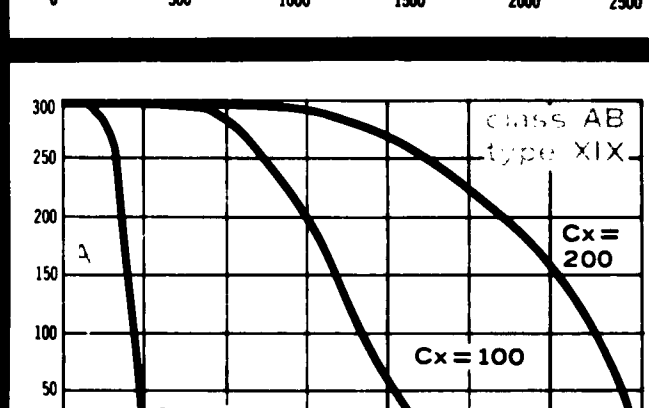

class EF type VIII
E
50 Kc
125 Kc
250 Kc
F
500
400
300
200
100
0
1000
2000
3000
4000
5000
6000
7000

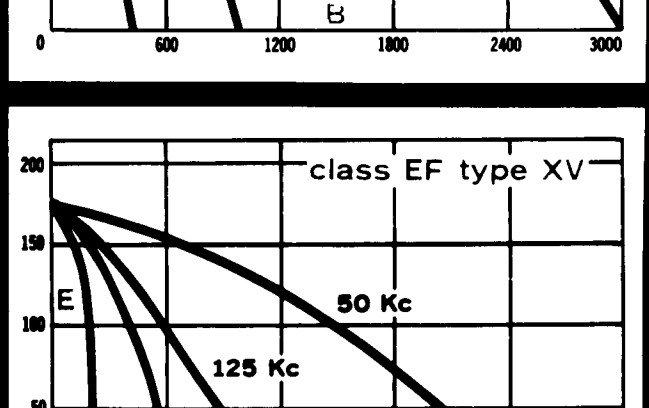

class AB type XII
A
Cx=400
Cx=100
Cx=0
B
160
120
80
40
0
400
800
1200
1600
2000
2400
2800

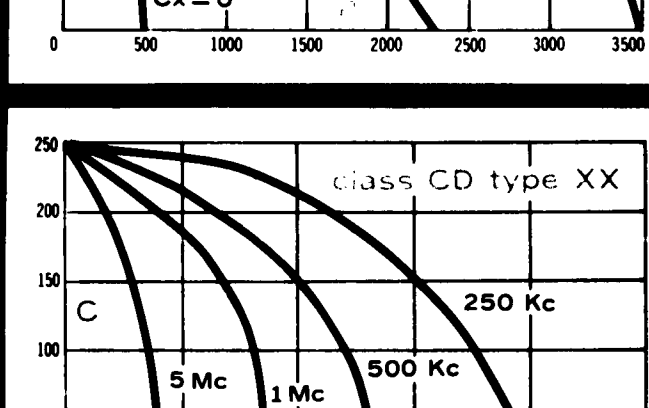

class AB type XIII
A
B
50 Kc to 125 Kc
250 Kc
0
15
30
45
60
75
100
200
300
400
500
600

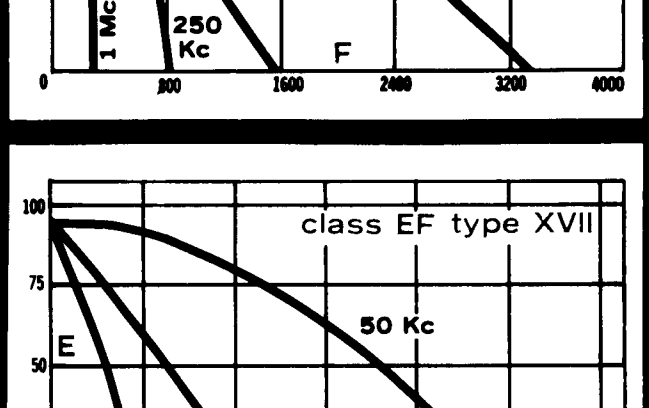

class AB type XVIII
A
B
50 Kc
125 Kc
250 Kc
0
60
120
180
240
300
360
500
1000
1500
2000
2500

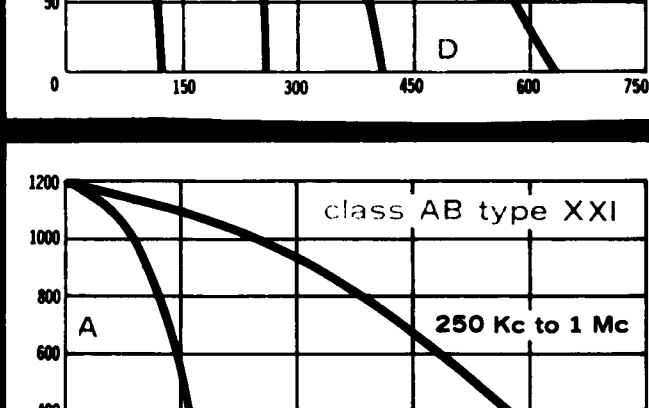

class AB type XIV
A
B
50 Kc
125 Kc
250 Kc
0
20
40
60
80
100
120
600
1200
1800
2400
3000


class AB type XIX
A
Cx = 200
Cx = 100
Cx = 0
0
50
100
150
200
250
300
500
1000
1500
2000
2500
3000
3500


class EF type XV
E
F
50 Kc
125 Kc
250 Kc
1 Mc
0
50
100
150
200
800
1600
2400
3200
4000


class CD type XX
C
D
250 Kc
500 Kc
1 Mc
5 Mc
0
50
100
150
200
250
150
300
450
600
750


class EF type XVII
E
F
50 Kc
125 Kc
250 Kc
0
25
50
75
100
400
800
1200
1600
2000
2400


class AB type XXI
A
B
250 Kc to 1 Mc
0
200
400
600
800
1000
1200
200
400
600
800
1000

USE OF EMITTER FOLLOWERS

Emitter followers are used to increase the load-driving capability of the drive unit or to provide better circuit isolation between the drive unit and the load unit. **PNP** emitter followers such as T-111 are generally used to drive DC logic or other resistive loads. When driving capacitative loads (one that has a capacitor in series with its input and therefore requires a pulse to drive it) with PNP emitter followers, connect a 5.6KΩ resistor from the output of the emitter follower to the +12 volt supply. This is done to lower the output impedance of the emitter follower for positive-going signals and, thus, increase its driving ability for positive pulses.

NPN emitter followers such as T-114 are generally used to drive capacitative loads because they have a minimum output impedance for positive pulses or positive-going signals. They are also good for driving control inputs of Pulse "And" gates and control inputs of Shift Registers and Gated flip-flops.

Use of an emitter follower will increase the load-driving capability of a given driver by a factor of 2 to 2.5. Of course this does not apply if the driver already has an integral emitter follower.

EXAMPLES:

Frequency	Drive Unit	Emitter Follower	Permissible Load
250Kc	T-101B	NONE	4 T-102A
250Kc	T-101B	T-114	8 to 10 T-102A
250Kc	T-104	NONE	2 T-106 (Direct Input)
250Kc	T-104	T-111	4 T-106 (Direct Input)

One note of caution: When the emitter follower being driven is, in turn, used to drive DC logic or control inputs of pulse logic, lighter loading is most desirable so that the driving circuit output levels will not be detrimentally lowered in amplitude. Consider, for example, the case where a heavily loaded unit with a 6 volt output and a lightly-loaded unit with an 8 volt output are both connected into the same logic circuit. In this case, it is possible to get an undesired 2 volt pedestal which may trigger succeeding circuits.

Input circuit differentiation can be accomplished in a conventional fashion with a series capacitor and a resistor returned to a bias of proper value to establish the quiescent output voltage. When this is done, care should be taken to keep operating conditions within the maximum signal amplitude allowed.

LOADS ON BOTH OUTPUTS OF FLIP-FLOPS

When the drive unit is a flip-flop without an emitter follower built in on the output, the drive capability shown on the drive characteristic curve is the total combined load that can be driven by both outputs of the flip-flop. This total load can also be driven by either output singly.

USE OF PULSE "AND" GATES

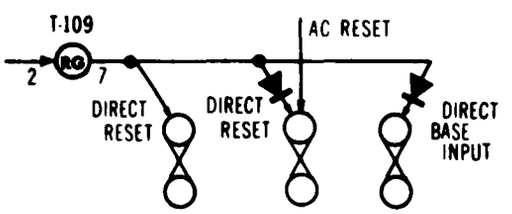
Pulse "And" Gates such as T-410A and T-630 are not recommended as loads for CD drivers because of rise-time deterioration. Additionally, due to low output amplitudes, Pulse "And" Gates are poor driving units and should be used to drive flip-flops only. These flip-flops will then, in turn, have only **half of their normal driving ability.** For example, the usual permissible load for a T-101B is 4 T-102A's but, when the T-101B is driven by a T-410A, the driving ability of the T-101B is reduced to 2 T-102A's; one-half its normal driving ability.

USE OF RESET GENERATORS

Reset Generator T-109 is used for **direct set** (when this terminal is available) or **direct reset** of flip-flops. With a nominal −3VDC applied at the input of the T-109, the output of the T-109 is approximately 0VDC; the level used for resetting. When a T-109 is connected to direct reset inputs of flip-flops and −3VDC is applied to the T-109, pin-8 outputs of the flip-flops will be held at −3VDC. However, if trigger pulses are applied to the flip-flops while they are being held reset, pulses may appear at the pin-7 outputs and detrimentally trigger subsequent circuits.

When T-109 is used to reset flip-flops at **direct base inputs,** an external diode must be used to isolate the relatively low output impedance of the T-109 from the unit being reset at times other than "reset time." Connect the cathode of the diode to the base input and the anode of the diode to the T-109 output. This diode is internal on units which have direct reset inputs.

If the direct reset input is used **in addition** to the AC reset input, then it is necessary to use an isolating diode between the T-109 output and the AC reset of these units. Otherwise, a pulse at the AC reset input will "see" a low-impedance path through the T-109 and not trigger the flip-flop properly.

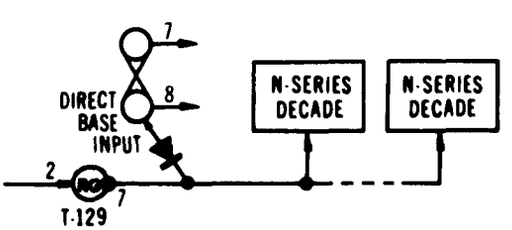


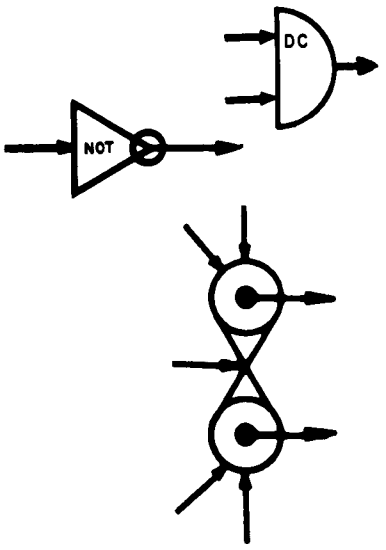
Reset Generator T-129 is designed to reset N-Series Decade Counters; a −3VDC input to T-129 causes approximately −4VDC out of the T-129. This −4VDC is the level used for resetting N-Series units.

CAUTION

When resetting less than 3 decades or less than 10 flip-flops, connect a 1KΩ resistor in series with the output of the T-129. This resistor is necessary to limit the reset current for light loads.

T-129 can also be used to reset flip-flops which have direct base inputs. In this case, connect a diode between the output of the T-129 and the base input of the flip-flop with the cathode of the diode connected to the T-129 (this diode is internal in the decades). Now, a −3VDC input to the Reset Generator causes the **pin-7** output of the flip-flop(s) to be held at −3VDC. (Note that this is the opposite of what happens when T-109 is used.) Once again, if trigger pulses are applied to the flip-flop(s) while they are held reset, pulses may result at the pin-8 output and detrimentally trigger succeeding circuits. T-129 will hold N-Series decades reset even with pulses going into the trigger input of the decade but, if the decade has code outputs, the first stage output will show effects similar to those experienced with T-Series units.





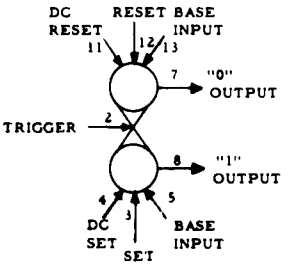
CIRCUIT SYMBOLS

Our system of circuit symbols is designed to provide rapid identification of circuit functions; to show direction of signal flow; and to accommodate combinations of circuit symbols in a logical manner for purposes of indicating internal gating, gradations of drive ability, etc. Use of these symbols will give a full measure of benefits:

1. **Engineering sketches made with these symbols are essentially equipment schematics, so design changes are simplified and final drafting is materially speeded up.**
2. **Technicians familiar with these symbols can expedite their construction and repair work.**
3. **Draftsmen using these symbols can produce final drawings at reduced cost. (Symbol templates are available as a further drafting aid.)**

The following paragraphs define the symbols used in literature and drawings produced by the Engineered Electronics Company. Signal connections to each symbol are numbered to correspond with pin connections on the module. Internal connections can be determined, if desired, by reference to specification sheets in the catalog. Specification sheets are quickly located by referring to circuit symbols and circuit numbers printed next to the circuit schematic.

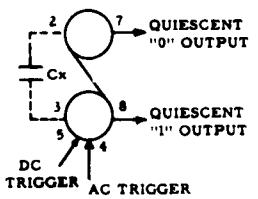
BISTABLE ELEMENTS — Flip-flops are symbolized as shown below. The two circles represent the two active circuit elements. The various inputs enter the symbol in a manner which represents how they affect the circuit. For example, an 8-volt positive-going pulse or voltage step applied to pin 12 resets the flip-flop; the "1" output (pin 8) rises to −3 volts and the "0" output (pin 7) falls to −11 volts. Once the flip-flop is in a reset state, any further reset inputs do not affect the flip-flop. An 8-volt positive-going pulse or voltage step applied to pin 3 sets the flip-flop; the "1" output falls to −11 volts and the "0" output rises to −3 volts. Positive pulses or voltage steps applied to the trigger input (pin 2) cause the pin-7 and pin-8 outputs to change level; if the flip-flop is in a set state, a pulse at pin 2 resets the circuit; if the flip-flop is in a reset state, a pulse at pin 2 sets the circuit.



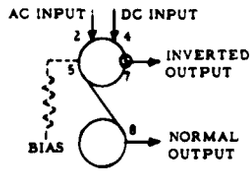
NOTE: Throughout this book, where input signals are identified as "pulse," the signals can be replaced by voltage steps when the input terminal is AC-coupled. In other words, AC-coupled inputs will generally differentiate the input signal.

If a given flip-flop has a direct-coupled input, the input lines are slanted from the left side of the symbol as shown at pin 4 (d-c set) and pin 11 (d-c reset). If a given flip-flop has an input connection direct to the base of one of the flip-flop transistors, the input lines are slanted from the right to the symbol as shown at pins 5 and 13.

MONOSTABLE ELEMENTS — One-Shots and Squaring Amplifiers are symbolized as shown. The two circles again represent the two active circuit elements but only one line joins the circles. In the case of the one-shot, an external capacitor connection is required and is thus shown in dotted lines. The two one-shot outputs are identified in terms of their untriggered state. That is, the pin-8 ouput rests at −3 volts and the pin-7 output rests at −11 volts. When a trigger pulse is applied at either pin 4 (a-c trigger) or pin 5 (d-c trigger), the pin-8 output falls to −11 volts and the pin-7 output rises to −3 volts for a period of time equal to the RC time constant of the circuit. At the end of this time, both outputs return to their quiescent level.

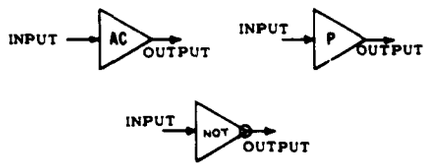


The squaring amplifier is a modified Schmitt trigger circuit which remains in one output state until the input exceeds a trigger level. When this level is exceeded, the circuit rapidly switches to a second output state and remains in this second state until the input voltage falls below the trigger level. Two opposite-state outputs (pin 7 and pin 8) are generated. When the circuit is in an untriggered state,



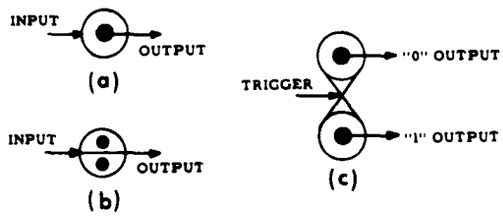
the pin-8 output rests at −11 volts and the pin-7 output rests at −3 volts. When the circuit is triggered by a positive-going voltage, the pin-8 output rises to −3 volts and the pin-7 output falls to −11 volts. The small open circle at output pin 7 represents the fact that this output is essentially an inversion of the pin 2 or pin 4 input. An external bias voltage applied at pin 5 can be used to control the threshold level at which the circuit is triggered and is thus shown in dotted lines.

AMPLIFIERS AND INVERTERS — Amplifiers and Inverters are represented by equilateral triangles pointed in the direction of signal flow. The exact function of any given device is indicated by markings within the triangle. For example, AC indicates an a-c amplifier, P indicates a pulse amplifier, NOT indicates a logic inverter, etc.



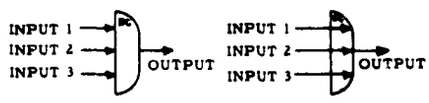
Where applicable, inversion is indicated by a small circle superimposed over the output as shown with the logic inverter symbol.

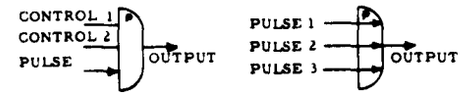
EMITTER FOLLOWERS — NPN and PNP emitter followers are represented as shown in (a) below. Note that no discrimination is made between the two types. Complementary emitter followers, which are a paralleled combination of NPN and PNP transistors, are symbolized as shown in (b).



Frequently emitter followers are incorporated as an integral part of a circuit module in order to provide greater drive capability. In this case, the emitter follower symbol is combined with the particular circuit symbol in question. A flip-flop with integral emitter follower outputs is shown in (c) above.

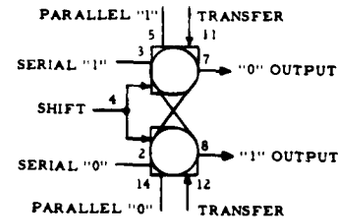
LOGIC ELEMENTS — "Or" and "and" gates are represented by a semi-ellipse. Input signal lines terminate at the major axis of the ellipse to represent an "and" gate and are carried into the symbol terminating at the convex side to represent an "or" gate. Output lines contact the center of the convex side.



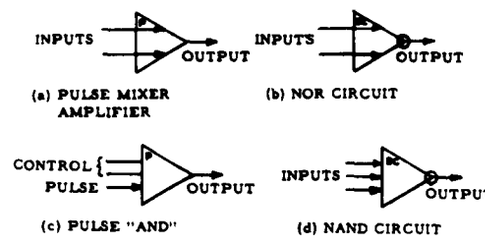


Note that a discrimination is made between d-c gates and pulse gates. The letters DC and P are used to designate the two types of gate and, in addition, control inputs to a pulse "and" gate do not have any arrowheads.

COMBINED SYMBOLS — If a circuit module consists of a combination of basic circuits, the basic symbols are synthesized to show this combination. For example, a gated flip-flop containing 4 integral pulse "and" gates is shown below. These gates are represented by a box enclosing the affected element of the flip-flop. The circuit shown is useful as one element of a shift register where parallel-form data is gated into the register by transfer pulses at pins 11 and 12. If a chain of these flip-flops is used, data from one element can be serially shifted to the next element in the register by shift pulses applied at pin 4.



Another example of combined circuit symbols is the convention used for pulse mixer amplifiers, NOR circuits, pulse "and" gates which contain amplifiers, and NAND circuits. The amplifier symbol is used to represent amplification accomplished by the circuit and the inputs are either terminated at the base of the triangle ("and") or carried into the triangle ("or") in a manner similar to that used for logic elements. In the case of NOR (not "or") and NAND (not "and") circuits, an open circle is superimposed on the output to represent logic inversion occurring in the circuit.



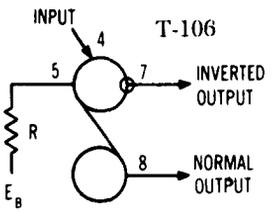
POWER CONNECTIONS — Power connections are not shown on the circuit symbols. These connections are eliminated for purposes of clarity and simplicity, but may be quickly checked by reference to the specification sheets. In order to simplify bus-wiring of sockets, uniform pin connections are used as previously described, wherever practicable. However, the number of pins required for signal connections varies considerably from unit to unit and, in some cases, the circuit design makes it impossible to reserve pin connections for power. CHECK SCHEMATICS BEFORE WIRING SOCKETS TO AVOID ERRORS AND POSSIBLE DAMAGE TO UNITS.

T circuit data section

This section contains four specific types of data for each circuit: general description, table of specifications, schematic drawing and symbol.

Units are grouped by circuit type and function and groups are in alphabetical sequence. Location and/or comparison of specific units can be made by the most expedient route for the immediate need: the Table of Contents, which begins on page 2, is arranged according to circuit function and lists key circuit data, such as speed and number of inputs for the Logic Circuits, voltage characteristics for the Relay Drivers, etc. A Cross Index by module number appears on page 4. Finally, the section itself is arranged in alphabetical sequence:

SQUARING AMPLIFIERS
T-106, T-306, T-312



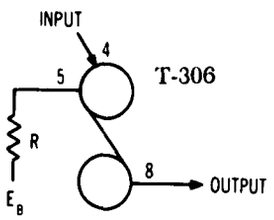
T-106 ONLY

(1.) $R = \frac{-(E_B + 2.5)\ 10}{E_3 + 2.5}$

(2.) $E_1 = \frac{-(E_B + 2)\ 10}{R} - 2$

(3.) $E_2 = \frac{(E_B + 3)\ 10}{R} - 5$

(4.) When bias supply voltage is positive, the following must be true: $1.5 > \frac{(E_B + 9)}{R}$

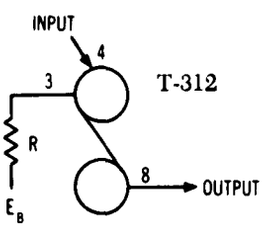


T-306 ONLY

(5.) $R = \frac{-(E_B + 3)\ 10}{E_3 + 6}$

(6.) $E_1 = \frac{-(E_B + 3)\ 10}{R} - 3.5$

(7.) $E_2 = \frac{-(E_B + 3)\ 10}{R} - 8.5$



T-312 ONLY

(8.) $R = \frac{-(E_B + 3)\ 66}{6E_3 + 29}$

(9.) $E_1 = \frac{-(E_B + 2)\ 11}{R} - 3$

(10.) $E_2 = \frac{-(E_B + 3)\ 11}{R} - 7$

DESCRIPTION

These units are basically modified Schmitt Trigger circuits which remain in a given output state until the inputs exceed a trigger level. At this time, the circuits rapidly switch to a second output state and remain in this second state until the input signal returns below the trigger level. The trigger level is adjustable by means of a bias voltage applied to pin 5 of T-106 and T-306 and to pin 3 of T-312. For example, in a system using our standard signal levels of −3 and −11 volts, a threshold of −6.5VDC can be established for T-106 by connecting a 47KΩ resistor from pin 5 to +12VDC.

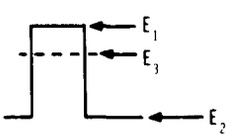
These circuits are typically used for such purposes as waveform restoration, signal level shifting, "Not" circuits, squaring sinusoidal or nonrectangular inputs, pulse amplification and DC level detecting (although they are not as sensitive as T-172 for this latter application).

SIGNAL LEVEL SHIFTING

Squaring Amplifiers T-106 (0 to 250 Kc), T-306 (0 to 5 Mc) and T-312 (0 to 1 Mc) can be used to convert other system signal levels to T-Series voltage levels by applying a suitable bias voltage. This bias voltage adjusts the threshold level of the amplifier to adapt it for use with input signals having minimum amplitudes equal to or greater than the amplitudes called out in unit specifications.

If an input signal is more positive than the most positive level called out and more negative than the most negative level called out, a bias voltage is not required and the units operate around their normal threshold levels. If, however, the input signal excursion does not fall within these limits, a bias voltage is used to select a convenient threshold level. This level should be approximately 1 volt more positive than the mid-point of the input signal for maximum reliability and noise rejection. If the threshold level is to be more negative than −2.5 volts, use a +12-volt bias supply (E_B); if the level is to be more positive than −2.5 volts, use a −12-volt bias supply voltage.

The relationships between bias resistance R (in KΩ), bias supply voltage E_B (in volts), and maximum and minimum input excursions (in volts) are listed in equations (1) through (10) . . . Equations (1) through (4) apply when T-106 is used, equations (5) through (7) apply when T-306 is used, and equations (8) through (10) apply when T-312 is used.



E_1 Minimum most-positive excursion of input signal.

E_2 Minimum most-negative excursion of input signal.

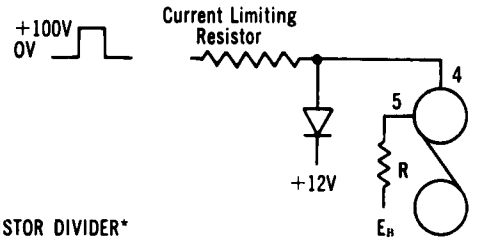
E_3 Threshold Level.

The following paragraphs illustrate two examples of level conversion using Squaring Amplifier T-106.

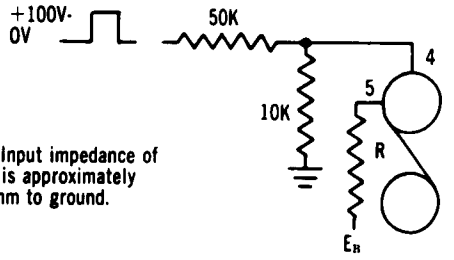
Converting Large Input Signals.

If the input signal has a 20-volt swing or greater, a clamping diode or resistor voltage divider should be used as shown.

DIODE CLAMP



RESISTOR DIVIDER*



*Note: Input impedance of T-106 is approximately 15K-ohm to ground.

In the sample shown, the signal into the T-106 will be approximately 0 volts to +10 volts and a threshold level of +6 volts should be selected. Since the threshold level is more positive than −2.5 volts, a −12-volt bias voltage should be used.

To find the bias resistance (R) required to obtain a threshold of +6 volts, use equation (1):

$$R = -\frac{(E_B + 2.5)\,10}{E_1 + 2.5} = -\frac{(-12 + 2.5)\,10}{6 + 2.5}$$

$= 11$ KΩ. (Use 12 K resistor)

Check to assure that the signal has enough swing to trigger the T-106. The input signal must swing more positive than E1 and more negative than E2.

$$E_1 = -\frac{(E_B + 2)\,10}{R} - 2 = -\frac{(-12 + 2)\,10}{12} - 2$$

$= +6.3$ volts

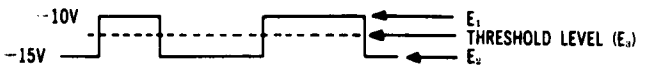
$$E_2 = -\frac{(E_B + 3)\,10}{R} - 5 = -\frac{(-12 + 3)\,10}{12} - 5$$

$= +2.5$ volts

Thus, the signal to the T-106 must shift at least from +2.5 volts to +6.3 volts. Since the signal applied swings from 0 v to +10 v, there is more than enough to trigger the T-106.

Converting Small Input Signals.

The same method is used to select bias resistance when small input signals are applied, however, the value of R becomes more critical. For example, assume an input signal which shifts from −15 volts to −10 volts.



Select a threshold level of −11.5 volts (1 volt more positive than the −12.5 volt midpoint of the input signal). Since the threshold level is more negative than −2.5 volts, a +12-volt bias voltage should be used as E_B. Use equation (1) to determine the value of bias resistance required.

$$R = -\frac{(E_B + 2.5)\,10}{E_1 + 2.5} = -\frac{(+12 + 2.5)\,10}{-11.5 + 2.5}$$

$=16$ KΩ (Use 15 K resistor)

Using equations (2) and (3), check to assure that the signal excursion is great enough to trigger the T-106.

$$E_1 = -\frac{(E_B + 2)\,10}{R} - 2 = -\frac{(12 + 2)\,10}{15} - 2$$

$= -11.3$ volts

$$E_2 = -\frac{(E_B + 3)\,10}{R} - 5 = -\frac{(12 + 3)\,10}{15} - 5$$

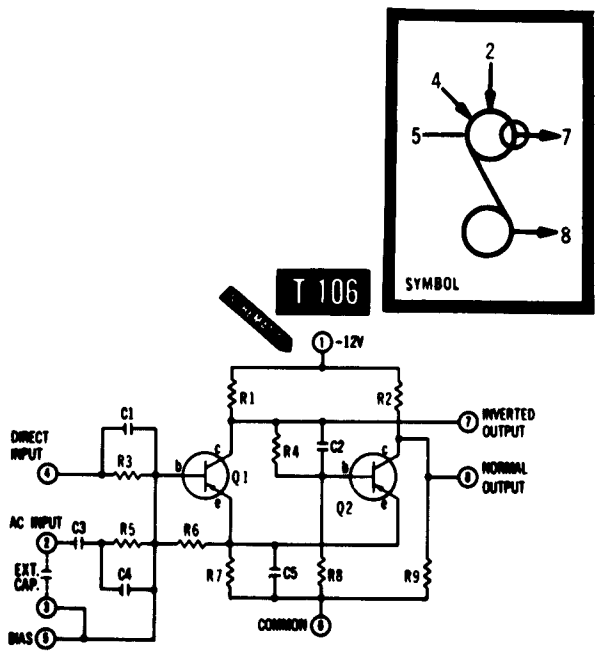
$= -15$ volts

Since the bias supply is positive, check to see if

$$\frac{E_B - 9}{R} < 1.5$$

$$\frac{12 - 9}{15} < 1.5$$

$$0.2 < 1.5$$



SQUARING AMPLIFIERS	T-106	T-306	T-312
INPUT			
SIGNAL FREQUENCY RANGE	0 to 500 Kc ††	0 to 5 Mc	0 to 1 Mc
MIN. AMPLITUDE TO CHANGE OUTPUT (level shift)	3V* (—2V to —5V)	5V (—8.5V to —3.5V)	4V (—7V to —3V)
RISE AND FALL TIMES REQUIRED	2 m sec max.	2 m sec max.	0.05 μsec min. 0.3 μsec max.
INPUT LOAD CHARACTERISTICS:			
A, B	50, 400	Pin 3: 65, 0 Pin 4: 40, 100	Pin 2: 0, 400 Pin 4: 50, 400
C, D	10, 100	Pins 3 & 4: 5, 25	Pin 2: 0, 100 Pin 4: 10, 100
E, F	50, 400	Pin 3: 65, 0 Pin 4: 40, 100	Pin 2: 0, 400 Pin 4: 50, 400
SIGNAL FREQUENCY RANGE	50 to 500 Kc † ††	100 Kc to 5 Mc ‡	250 Kc to 1 Mc
TRIGGER AMPLITUDE:			
Minimum	4V P-P	4.5V P-P	3V P-P
Nominal	5V P-P	6V P-P	6V P-P
Maximum	12V P-P	12V P-P	10V P-P
RISE AND FALL TIMES REQUIRED:	†	‡	0.05 μsec min. 1.0 μsec max.
INPUT LOAD CHARACTERISTICS:			
A, B	50, 400	(Pin 2) 35, 0	50, 400
C, D	10, 100	(Pin 2) 5, 25	10, 100
E, F	50, 400	(Pin 2) 35, 0	50, 400
OUTPUT			
AMPLITUDE (level shift)	8V (—11 to —3V)	8V (—11 (+0.5 or —1.0) to —3 (+0.3 or —1.0) V)	8V (—11 (±1.0) to —3 (±1.0) V)
RISE TIME (under typical load)	Pin 8: 0.6 μsec Pin 7: 0.8 μsec	6 to 40 nsec	0.2 μsec max.
LOAD DRIVE CHARACTERISTICS	AB type XIV	CD type XX	AB type X
POWER REQUIRED			
—12 VDC ±10%	5.0 ma	18 ma max.	16 ma max.
OPERATING TEMPERATURE RANGE	—45 to +65 C	—55 to +71°C	—55 to +71°C

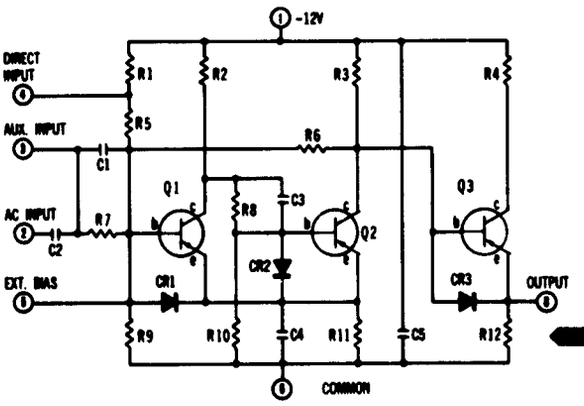
* For 8V level shift from —11 to —3V, connect external 47 KΩ resistor from Pin 5 to +12V supply.

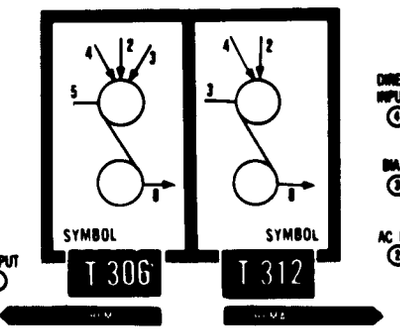
† For sine-wave inputs at frequencies lower than 50 Kc, add external capacitor between pins 2 & 3 as follows:

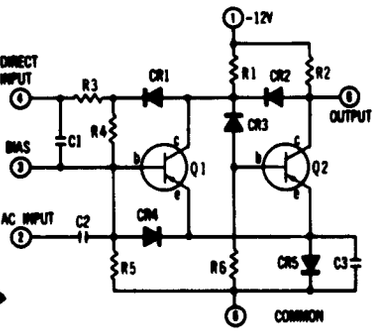
Freq.	Capac.
1 to 5 Kc	0.1 uf
5 to 25 Kc	0.022 uf
25 to 50 Kc	0.0047 uf

‡ Low-frequency range can be extended by connecting external capacitor between pins 2 & 3.

†† Operating frequency may be extended to 1 Mc with 6V P-P sine-wave input and emitter-follower buffering on output.







AMPLIFIERS
T-108 (LINEAR), T-305 (VIDEO), T-118 (PULSE)

DESCRIPTION

T-108 is a linear amplifier which can be used to amplify low-level input signals to a level usable by T-Series circuits. Inputs can be sine waves, square waves, pulses, or other complex wave forms, provided the frequency components of the signal are within the response range of the amplifier. Input sources include voltage pick-ups, low-level transducers, etc. Chart I illustrates the basic input impedance limits of T-108.

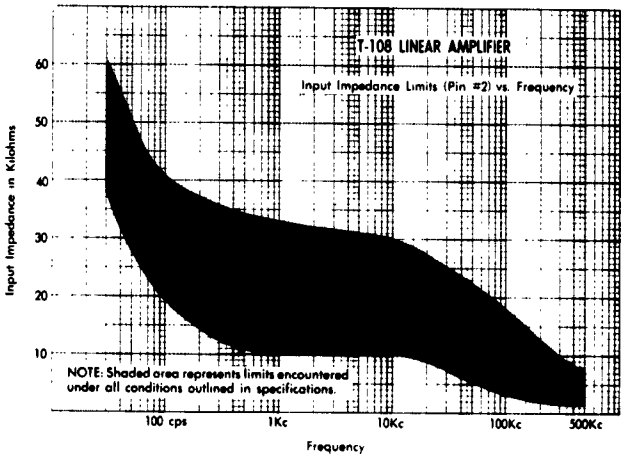


Chart I — Input Impedance Limits of T-108

Three fixed gain settings are selectable by jumpering pins; these gains are X10, X45, and X90 respectively. If no jumper is connected, a gain of X10 is realized. Gains of X45 and X90 are realized when a jumper is connected from pin 3 to pin 5 in the former case and from pin 3 to pin 7 in the latter case. Improved low-frequency response can be achieved by coupling inputs via a large capacitor to the pin-4 input and connecting a large bypass capacitor from pin 3 to pin 6. Chart II illustrates typical frequency response curves for T-108.

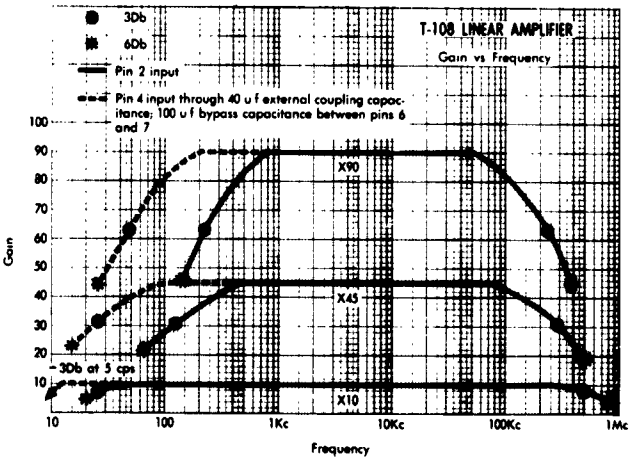


Chart II — Frequency Response of T-108

T-305 is also a linear amplifier but, because its frequency response extends to 10Mc, it is referred to as a video amplifier. Because the response of this amplifier exceeds 10Mc and because the output is in phase with the input, careful use of RF techniques in external wiring is mandatory. For example, input and output leads should be either shielded or widely separated from one another and as short as possible; power supply leads should be as short as possible and high-frequency by-passed where necessary; ground return should be carefully selected to reduce ground loops to a minimum. Pin 9 should be jumpered to pin 6 by a short piece of straight buss wire directly across the bottom of the socket. The best grounding scheme is to use pin 6 for power supply and input signal ground and pin 9 for output signal ground.

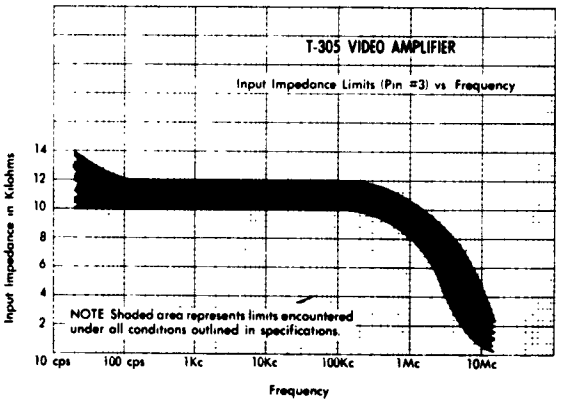


Chart III — Input Impedance Limits of T-305

Three fixed gain settings are also selectable for T-305 by jumpering pins; these gains are X10, X31.6, and X100. When no jumper is connected, a gain of 10 is realized. Gains of 31.6 and 100 are realized when a jumper is connected from pin 4 to pin 7 in the former case and from pin 4 to pin 5 in the latter case. Chart IV presents typical response curves for T-305 at these three gain settings.

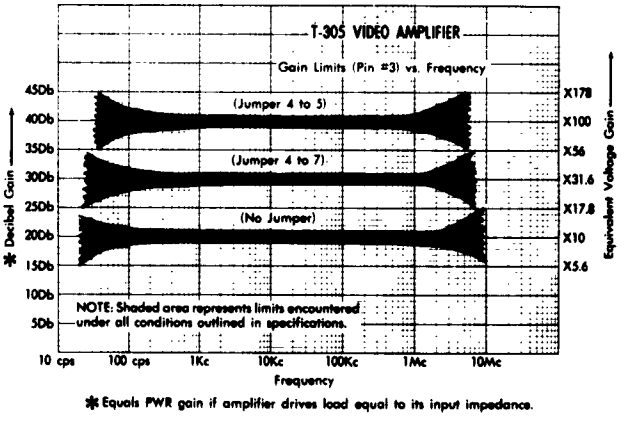


Chart IV — Frequency Response of T-305

T-118 is a transistorized Pulse Amplifier used to produce standardized positive-going pulses with a sharp rise time. The input may be of deteriorated shape and low amplitude and can be either a positive-going pulse or voltage step.

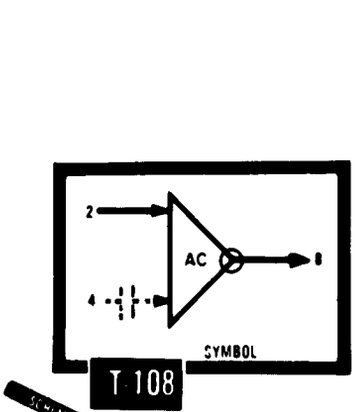
AMPLIFIERS	T-108 Linear Ampl	T-305 Video Ampl	T-118 Pulse Ampl
INPUT			
SIGNAL FREQUENCY RANGE	30 cps to 500 Kc	**20 cps to 10 Mc**	250 Kc max.
AMPLITUDE:			
For Linear Operation (depending on gain)	5 mV to 0.6V	**5 mV to 0.6V**	@ rise times up to 1 μsec:
Maximum	12V P-P†	**6V P-P*†**	5.5V pulse or step min.
INPUT IMPEDANCE	See Chart I	**See Chart III**	A - 10, B - 100 C - 8, D - 75 E - 10, F - 100
OUTPUT			
NOMINAL DC LEVEL	—7V	**—7V**	—11V
AMPLITUDE (undistorted)	6V P-P max.	**6V P-P max.**	min. 6V P-P pos. pulse
PHASE INVERSION	180	**none**	none
GAIN (See Description)	x10, x45, or x90	**x10, x31.6, or x100**	††
FREQUENCY RESPONSE	See Chart II	**See Chart IV**	—NA—
RANDOM OUTPUT NOISE	20 mV P-P	**50 mV P-P‡**	—NA—
OUTPUT IMPEDANCE	1 KΩ nominal	**500 Ω max (AC coupled)**	—NA—
LOAD DRIVE CHARACTERISTIC	1 T-106	**1 T-306 or T-312**	AB type XIII
RISE TIME	—NA—	**—NA—**	0.02 to 0.5 μsec
PULSE WIDTH	—NA—	**—NA—**	0.5 to 3.5 μsec
POWER REQUIRED			
—12 VDC ± 10%	2.5 ma	**15 ma**	2.5 ma quiescent 10 ma peak
OPERATING TEMPERATURE RANGE	—45 to + 65 C	**—54 to +71°C**	—45 to + 65 C

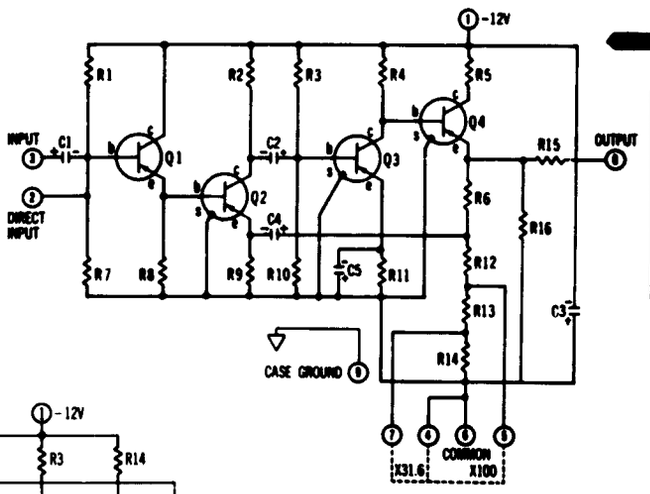
* Because of maximum voltage rating on input coupling capacitor, input signal levels at Pin 3 must always remain within the range of - 4 to + 45V. For signal levels beyond this range, use input Pin 2 and an external coupling capacitor with an adequate voltage rating. DC voltage at Pin 2 is - 4.5V (± 1.0V).

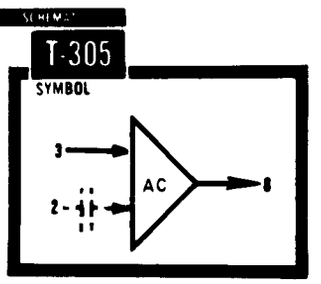
† Large transients can cause temporary blocking of subsequent low-level inputs.

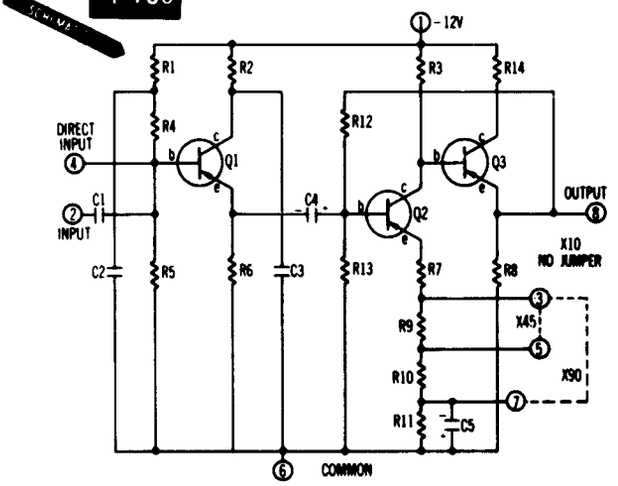
‡ Gain at X100, input terminated at 1 KΩ, Pin 9 grounded.

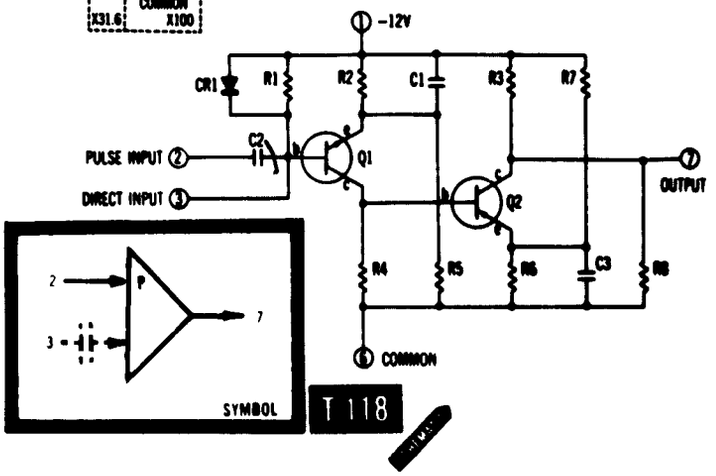
†† For signals having poor rise time, use Pin 3 input with an external capacitor of suitable size. The circuit will not respond to inputs of less than 1.5V amplitude regardless of rise time.











VOLTAGE COMPARATOR T-172

DESCRIPTION

T-172 is a voltage comparator designed to detect DC voltage levels in the range of −6 volts to +6 volts. Two inputs are used: a reference voltage and a voltage to be compared with this reference voltage. When the input signal is more positive than the reference voltage, the unit provides a −3-volt output; when the input signal is more negative than the reference voltage, the unit produces a −11-volt output.

T-172 can also be used as a level detector if the reference voltage input is grounded and a Zener diode and resistor network are used to pre-bias the input to the polarity opposite to that of the expected input. Values of resistance used should be as low as possible because source impedance will affect the sensitivity and temperature stability of the unit.

ELECTRICAL SPECIFICATIONS

INPUT:

Signal Frequency Range: 0 to 100Kc. For input frequencies from 100Kc to 250Kc, maximum level shift to cause full excursion of the output is 0.4V (±0.2V with respect to the reference voltage).

Input Signal: When signal is 0.1VDC greater than reference voltage, the output is nominally −3VDC; when signal is 0.1VDC less than reference voltage, the output is nominally −11VDC.

Minimum Input Level Shift to Cause Full Excursion of Output: 0.05VDC (Source impedance must be less than 100Ω for max. sensitivity.)

Input Load Characteristics:
A, B: 50, 0
C, D: 25, 200
E, F: 50, 0

OUTPUT:

Amplitude: −3VDC (±1) = signal exceeds reference voltage, −11VDC (±1) = reference exceeds signal voltage.

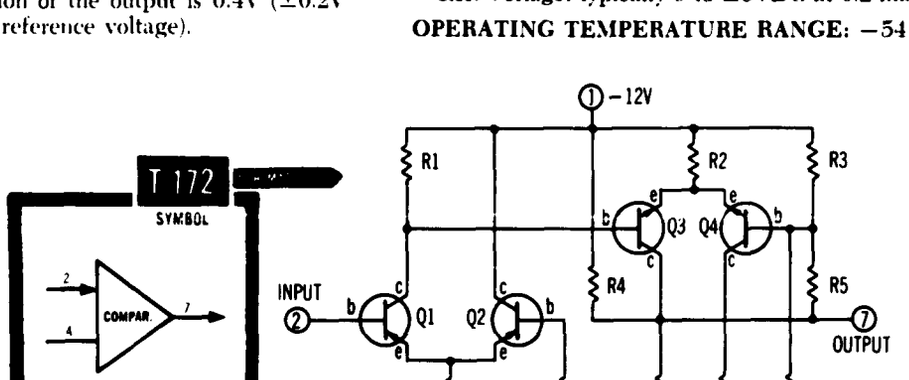
Rise Time: Less than 1 μsec for an input level shift from 0.5VDC below the reference to 0.5VDC above the reference with a rise time of less than 1 μsec.

Load Drive Characteristics: This is a CD type IX driver.

POWER REQUIRED:

−12VDC ±10%: 30 ma maximum
+12VDC ±10%: 6 ma maximum
Ref. Voltage: typically 0 to ±6VDC at 0.2 ma maximum

OPERATING TEMPERATURE RANGE: −54 to +71°C



DESCRIPTION

T-424A can be used as either a Half-Adder or a Half-Subtracter, depending on connection of an external jumper. Outputs, depending on this jumper connection, are Sum or Difference (Pin 7) and Carry or Borrow (Pin 8).

Half Adder Mode — The logic equations for a Half Adder are:

$$\text{Sum} \quad S = X\overline{Y} + \overline{X}Y$$
$$\text{Carry} \quad C = XY$$

A Full Adder is formed when a third input, "carry" from the next lowest significant digit, is added to the sum. Therefore, two Half Adders and an "Or" gate are necessary to make up a Full Adder. (See Truth Tables I and II.)

TRUTH TABLE I
Half Adder
(X plus Y = S)

X	0	1	0	1
Y	0	0	1	1
S	0	1	1	0
C	0	0	0	1

TRUTH TABLE II
Full Adder
(X plus Y plus C = S)

X	0	1	0	1	0	1	0	1
Y	0	0	1	1	0	0	1	1
C	0	0	0	0	1	1	1	1
S	0	1	1	0	1	0	0	1
C	0	0	0	1	0	1	1	1

Half Subtracter Mode—A Half subtracter provides Difference (D) and Borrow (B) outputs from two single-digit inputs (X minus Y). The logic equations for a Half Subtracter are:

$$\text{Difference} \quad D = X\overline{Y} + \overline{X}Y$$
$$\text{Borrow} \quad B = DY$$

Full Subtraction is performed when a third input, 'borrow" from the next lowest significant digit, is subtracted from (X minus Y). Two Half Subtracters and an "Or" gate are necessary to make up a Full Subtracter. (See Truth Tables III and IV.)

TRUTH TABLE III
Half Subtracter (X minus Y = D)

X	0	1	0	1
Y	0	0	1	1
D	0	1	1	0
B	0	0	1	0

TRUTH TABLE IV
Full Subtracter (X minus Y minus B = D)

X	0	1	0	1	0	1	0	1
Y	0	0	1	1	0	0	1	1
B	0	0	0	0	1	1	1	1
D	0	1	1	0	1	0	0	1
B	0	0	1	0	1	0	1	1

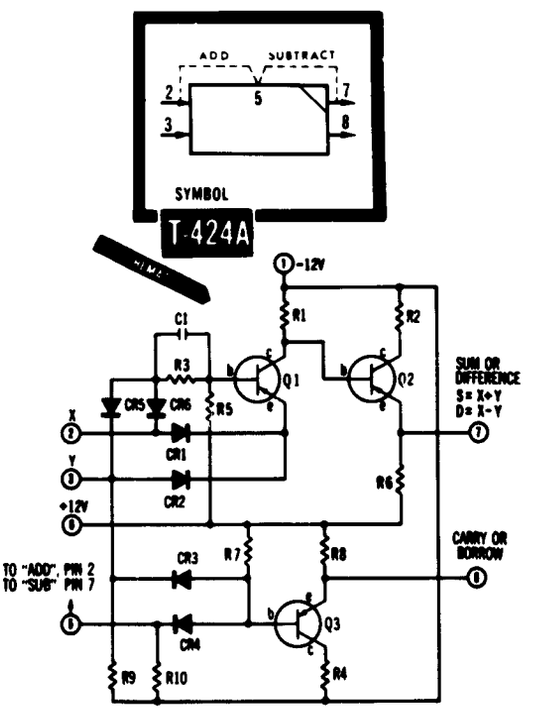
Note that the Sum and Difference equations are exactly alike; either can be formed by an "Exclusive-Or" gate. Carry and Borrow equations have similar form but different inputs. Either can be performed by an "And" gate if one of the inputs is connected to X for addition and to D for subtraction.

The time delay between input and output signal excursions (measured between half-amplitude points) is 1.5 microseconds maximum for one T-424A, or a total of 2.0 microseconds maximum for two cascaded T-424A units. In order to determine the maximum possible accumulated delay (T in μsec) through N cascaded T-424A units, use one of the following equations:

$$\text{if N is even:} \quad T = N$$
$$\text{if N is odd:} \quad T = N + 0.5$$

ARITHMETIC CIRCUIT	T-424A Half adder/subtracter
INPUT	
SIGNAL FREQUENCY RANGE	0 to 250 Kc
SIGNAL LEVELS (nominal):	
Binary "1"	—3 VDC
Binary "0"	—11 VDC
RISE TIME	0.1 to 1.0 μsec
FALL TIME	0.1 to 2.5 μsec
INPUT LOAD CHARACTERISTICS:	
A, B	80, 0
C, D	5, 25
E, F	80, 0
OUTPUT	
AMPLITUDE (nominal)	—3 VDC = "1", —11 VDC = "0"
RISE TIME (depending on input rise & fall time)	0.1 to 1.0 μsec
LOAD DRIVE CHARACTERISTICS	CD type IX
POWER REQUIRED	
—12 VDC ±10%	8 ma
+12 VDC ±10%	8 ma
OPERATING TEMPERATURE RANGE	—54 to + 71 C

table continued on next page



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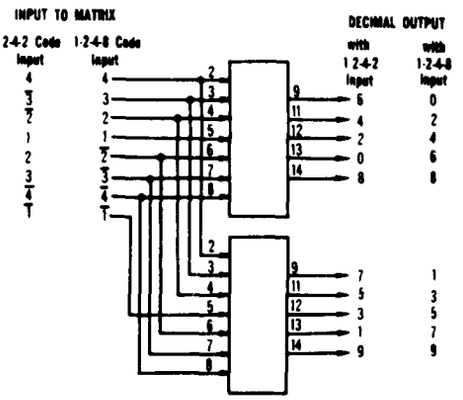
T-628 is basically a code converter intended for use in pairs to convert a 1-2-4-2 or a 1-2-4-8 binary-coded-decimal input to a 10-line decimal output (0-9) for driving relay drivers. The matrix is arranged so that emitter followers are not required on either input or output. Relay Drivers such as T-120, T-121, and T-128 can be loaded on all outputs simultaneously.

NOTE: T-628 cannot be used with the Digital System Breadboard Equipment because pin 9 is wired to ground on the T-927 System Development Panels.

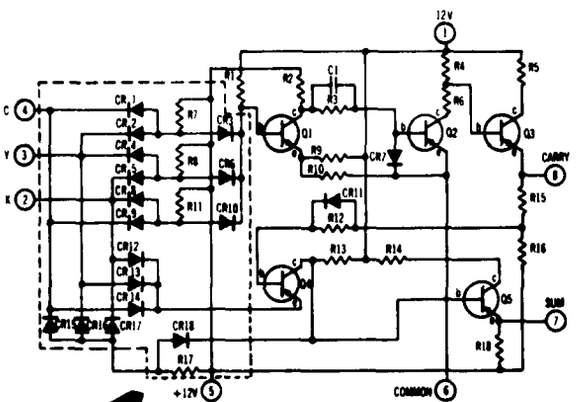


CONNECTIONS NECESSARY FOR CODE CONVERSION

T-441 is a complete Full Adder in one package. Three inputs (one each for the addend X, the augend Y, and a carry C from the previous digit of lower significance) cause Sum and Carry outputs as shown in Truth Table II. A built-in amplifier circuit minimizes level shift and, thus, eliminates need for restoring circuits in the carry propagation path of a system.

The delay from input to carry output (pin 8) is 1.7 μsec maximum for one T-441 operating under worst-case conditions. However, when two or more T-441 adders are cascaded (pin 8 of one to pin 4 of the next), the delay is approximately N microseconds, where N equals the number of T-441 units cascaded. Because of this delay, a characteristic of all logic circuits, the maximum frequency limit is reduced as the number of cascaded adders increases according to the equation:

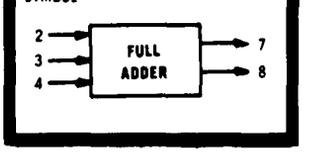
$$F_{max} = \frac{1}{3+N} \text{ (in Mc)}$$

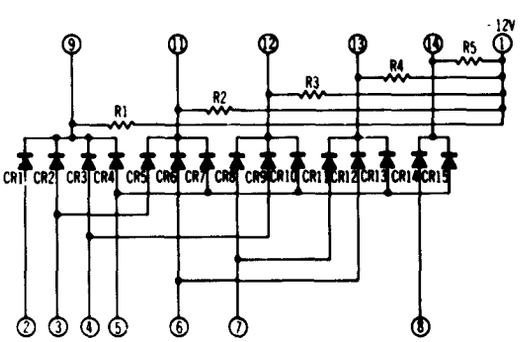


SCHEMATIC

T 441

SYMBOL





T 628

SYMBOL

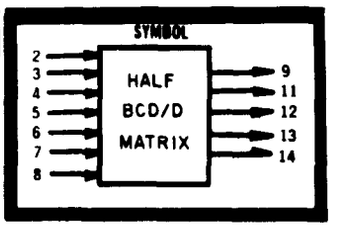


table continued from last page ARITHMETIC CIRCUITS	T-441 Full adder	T-628 Half BCD to decimal converter
INPUT		
SIGNAL FREQUENCY RANGE	0 to 250 Kc*	0 to 1 Kc
SIGNAL LEVELS (nominal):		
Binary "1"	—3 VDC	—11 VDC
Binary "0"	—11 VDC	—3 VDC
RISE TIME	0.1 to 1.0 μsec	— NA —
FALL TIME	0.1 to 2.5 μsec	— NA —
INPUT LOAD CHARACTERISTICS:		
A, B	50, 0	60, 0
C, D	5, 25	140, 0 ★
E, F	50, 0	60, 0
OUTPUT		
AMPLITUDE (nominal)	—3 VDC = "1", —11 VDC = "0"	—11 VDC = "1", —3 VDC = "0"
RISE TIME (depending on input rise & fall time)	Pin 7: 1.0 μsec max Pin 8: 1.0 μsec max or 20 times better than input (whichever is greater)	— NA —
LOAD DRIVE CHARACTERISTICS	CD type IV	Each output will drive one relay driver such as T-120, T-121, or T-128. ★
POWER REQUIRED		
—12 VDC ±10%	24 ma†	3.6 ma max.
+12 VDC ±10%	13 ma†	none
OPERATING TEMPERATURE RANGE	—54 to +71 C	—45 to +65°C

* See equation describing F max in Description.

† Excluding load current.

★ When connected to a driver capable of driving this additional load; i.e., a flip-flop already driving another flip-flop.

RELAY DRIVERS T-120 T-121 T-128 T-130 T-134 T-135 T-139 T-141 T-170 T-171

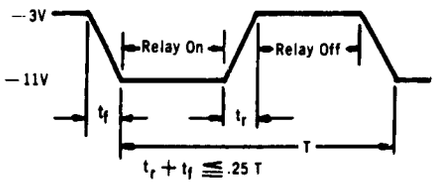
DESCRIPTION

These circuits are basically transistor switches that may be operated directly from the output of other T-Series circuits such as flip-flops, one shots or squaring amplifiers. Input signal levels required are −3VDC and −11VDC. As the specifications show, some units are activated at −3VDC and some are activated at −11VDC. Major variables to consider when selecting one of these units are maximum output current required and the output voltage level to be switched.

The most common application for these units is control of general-purpose relays. However, the units are equally useful for signal inversion and, or level changing. Dual units such as T-134 and T-135 also find use as Reset Generators in systems consisting of admixtures of T-Series and N-Series units.

When used to actuate relays, these units require protection against reverse surge voltages generated by the relay coil. To this end, diode clamping may be used across the coil as shown on the individual schematics. Diode requirements are: (1) Peak forward current = relay "on" current, and (2) peak inverse voltage = relay supply voltage.

INPUT WAVEFORM



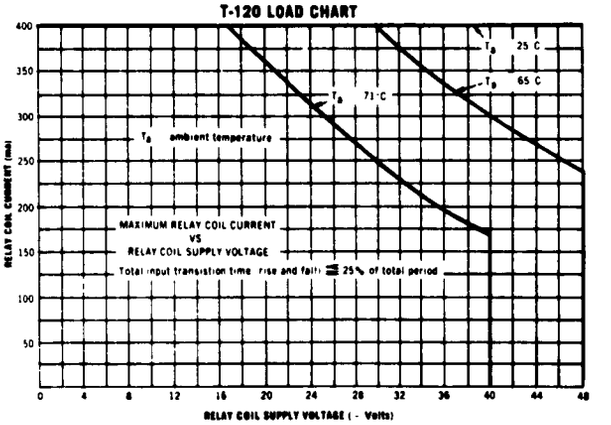
Absolute maximum value for t_r or t_f = 1 second.

t_f = fall time

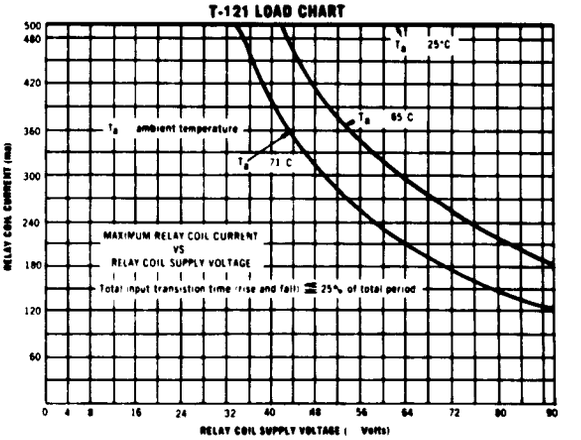
t_r = rise time

RELAY DRIVERS *table continued on next page*	T-120 −48V 500 ma Relay Driver	T-121 −90V 500 ma Relay Driver	T-128 −30V 500 ma Relay Driver
INPUT	††	††	††
SIGNAL FREQUENCY RANGE at max. output current	0 to 1 Kc	0 to 1 Kc	0 to 1 Kc
DC SIGNAL LEVEL TO ACTIVATE	−11V	−11V	−11V
DC SIGNAL LEVEL TO DEACTIVATE	−3V	−3V	−3V
MAX. SIGNAL CURRENT REQUIRED:			
at −11V, to a positive source	0.1 ma	0.1 ma	0.1 ma
at −3V, to a negative source	0.5 ma	0.5 ma	0.5 ma
MAX. RISE or FALL TIME†	1 sec	1 sec	1 sec
OUTPUT	‡	‡	
MAX. OUTPUT CURRENT	500 ma	500 ma	500 ma
MAX. OUTPUT SUPPLY VOLTAGE	−48V	−90V	−30V
RISE TIME, typical: longest of following:			
Time under max. load	6 μsec	6 μsec	6 μsec
% input fall time	10%	10%	10%
% input rise time			
FALL TIME, typical: longest of following:			
Time under max. load	6 μsec	6 μsec	6 μsec
% input fall time			
% input rise time	10%	10%	10%
CURRENT LEAKAGE through load in "off" condition and at maximum operating temperature:			
typical	1 ma	1 ma	1 ma
maximum	5 ma	5 ma	5 ma
POWER REQUIRED (exclusive of relay current)			
+12V (±10%) at	14 ma	14 ma	14 ma
−12V (±10%) at	30 to 45 ma	30 to 45 ma	30 to 45 ma
RELAY COIL SUPPLY maximum	−48V	−90V	−30V
OPERATING TEMPERATURE RANGE	−54 to +65°C ■	−54 to +71°C	−54 to +71°C

T-120 LOAD CHART



T-121 LOAD CHART



‡ Maximum output current available is dependent on relay voltage used; see load chart.

†† Max. frequency with relay load depends on relay capabilities

■ May be operated up to 71° C for relay voltages up to 40V.

† The sum of input rise and fall time must not be greater than 25% of total period.

continued on next page

RELAY DRIVERS *table continued from last page*	T-130 —28V, 1 amp. Relay Driver	T-134 —35V 100 ma Relay and indicator Driver* (dual)	T-135 —35V 100 ma Relay and Indicator Driver* (dual)	T-139 + 30V 400 ma Relay Driver	T-141 +45V 400 ma Relay Driver	T-170 + 35V 100 ma Relay and Indicator Driver (dual)	T-171 +35V 100 ma Relay and Indicator Driver (dual)
INPUT	††	††	††	††	††		
SIGNAL FREQUENCY RANGE at max. output current	0 to 1 Kc	0 to 50 Kc	0 to 50 Kc	0 to 1 Kc	0 to 1 Kc	0 to 50 Kc	0 to 50 Kc
DC SIGNAL LEVEL TO ACTIVATE	—11V	—11V	—3V	—3V	—3V	—11V	—3V
DC SIGNAL LEVEL TO DEACTIVATE	—3V	—3V	—11V	—11V	—11V	—3V	—11V
MAX. SIGNAL CURRENT REQUIRED:							
at —11V, to a positive source	0.4 ma	0.45 ma	0.2 ma	0.2 ma	0.2 ma	0.2 ma	0.5 ma
at —3V, to a negative source	0.5 ma	0.3 ma	0.5 ma	0.4 ma	0.4 ma	0.5 ma	0.2 ma
MAX. RISE or FALL TIME†	1 sec	1 msec	1 msec	1 sec	1 sec	1 msec	1 μsec (rise) 2 μsec (fall)
OUTPUT	•	•	•	•		•	•
MAX. OUTPUT CURRENT	1 amp	100 ma	100 ma	400 ma	400 ma	100 ma	100 ma
MAX. OUTPUT SUPPLY VOLTAGE	—30V	—35V	—35V	+ 30V	+45V	+ 35V	+35V
RISE TIME, typical: longest of following:							
Time under max. load	13 μsec	1 μsec	2 μsec	6 μsec	6 μsec	1 μsec	1 μsec
% input fall time	20%	20%		10%	10%	25%	
% input rise time			25%				25%
FALL TIME, typical: longest of following:							
Time under max. load	13 μsec	1 μsec	3 μsec	6 μsec	6 μsec	1 μsec	1 μsec
% input fall time			10%				25%
% input rise time	10%	20%		10%	10%	25%	
CURRENT LEAKAGE through load in "off" condition and at maximum operating temperature:							
typical	0.6 ma			0.02 ma	0.02 ma		
maximum	3 ma	0.1 ma	0.1 ma	0.3 ma	0.3 ma	0.5 ma	0.5 ma
POWER REQUIRED (exclusive of relay current)							
+12V (±10%) at	20 ma	12 ma	2.5 ma	30 ma max.	30 ma max.	12 ma max.	24 ma
—12V (±10%) at	20 ma	22 ma	14 ma	45 ma max.	45 ma max.	24 ma max.	24 ma
— 3V (±10%) at ★	110 ma						
RELAY COIL SUPPLY maximum	—30V	—35V	—35V	+ 30V	+45V	+ 35V	+35V
OPERATING TEMPERATURE RANGE	—54 to +65°C	—55 to +71 C	—55 to +71°C	—54 to + 65 C	—54 to +65°C	—55 to + 71 C	—55 to +71°C

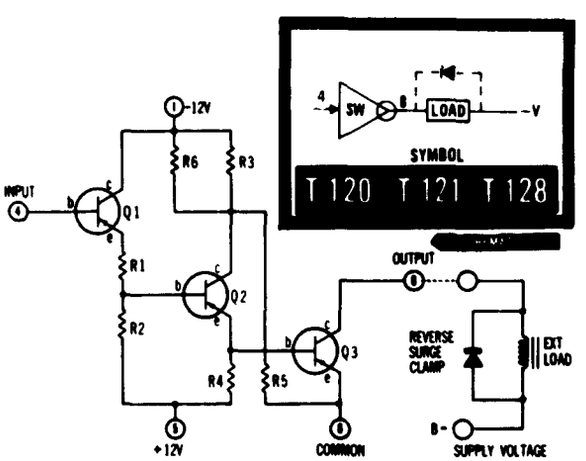
* Can also be converted to reset generator.

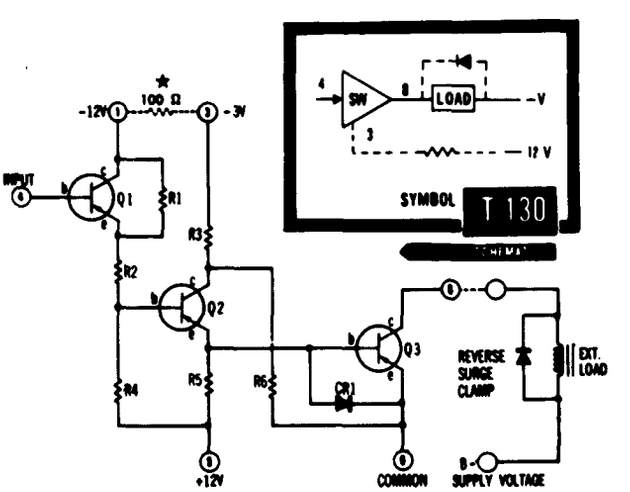
† The sum of input rise and fall time must not be greater than 25% of total period.

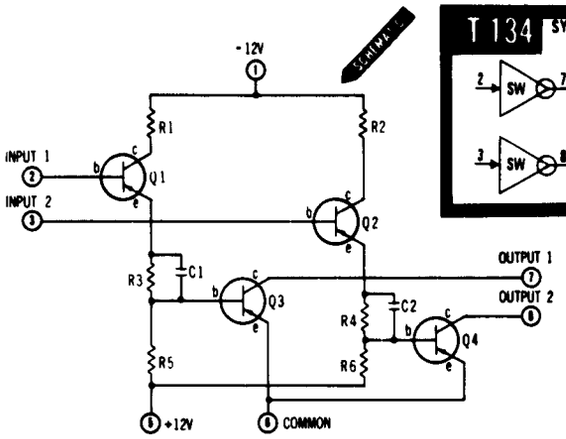
†† Max. frequency with relay load depends on relay capabilities.

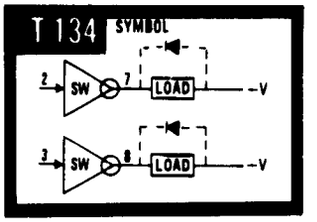
• No derating necessary over voltage and temperature range.

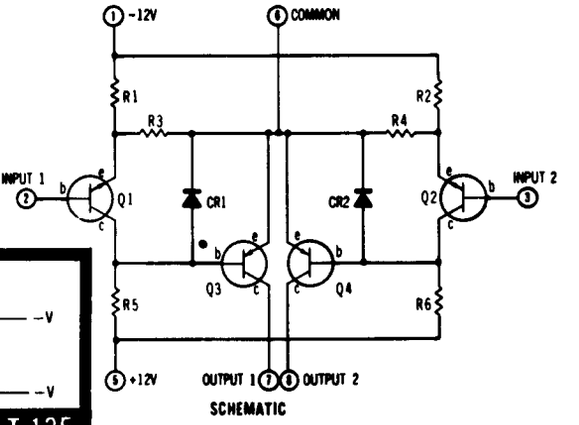
★ Can be derived from —12 V supply by connecting a 100 Ω, 2 watt resistor between pins 1 and 3.

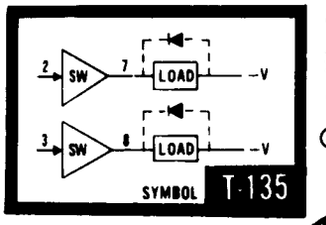


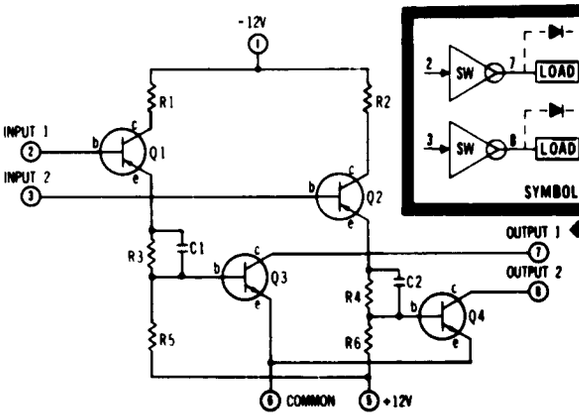



SCHEMATIC
-12V
R1
R2
INPUT 1
Q1
INPUT 2
Q2
C1
R3
Q3
OUTPUT 1
OUTPUT 2
C2
R4
Q4
R5
R6
+12V
COMMON

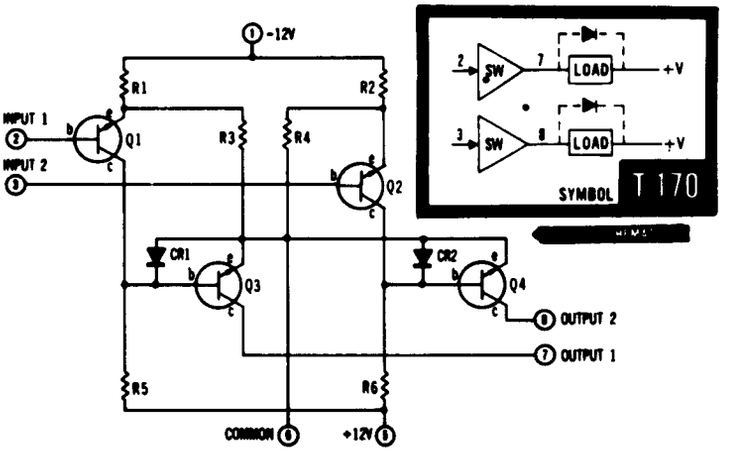

T 134
SYMBOL
SW
LOAD
-V


-12V
COMMON
R1
R2
R3
R4
INPUT 1
Q1
CR1
CR2
Q2
INPUT 2
Q3
Q4
R5
R6
+12V
OUTPUT 1
OUTPUT 2
SCHEMATIC

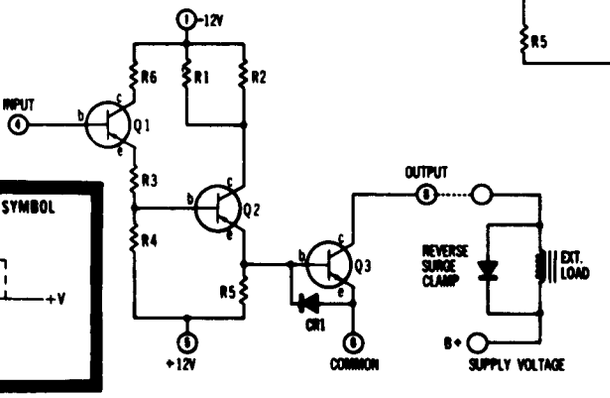

SW
LOAD
-V
SYMBOL
T-135

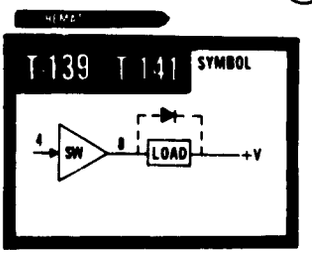

-12V
R1
R2
INPUT 1
Q1
INPUT 2
Q2
C1
R3
Q3
OUTPUT 1
OUTPUT 2
C2
R4
Q4
R5
R6
COMMON
+12V

SW
LOAD
+V
SYMBOL
T 171


-12V
R1
R2
INPUT 1
Q1
R3
R4
INPUT 2
Q2
CR1
CR2
Q3
Q4
OUTPUT 2
OUTPUT 1
R5
R6
COMMON
+12V

SW
LOAD
+V
SYMBOL
T 170


-12V
R6
R1
R2
INPUT
Q1
R3
Q2
R4
R5
Q3
CR1
OUTPUT
REVERSE SURGE CLAMP
EXT. LOAD
B+
SUPPLY VOLTAGE
+12V
COMMON


T-139
T-141
SYMBOL
SW
LOAD
+V

DRIVERS T-163, T-165, T-302

DESCRIPTION

T-163 is a transistorized driver containing five germanium transistors. An NPN emitter follower is used to drive four PNP emitter followers, each of which may be loaded in the same manner as T-111, T-112, or T-113 emitter followers. The typical driving unit into the T-163 is a T-101B or T-102A flip-flop, or equivalent.

The primary purpose of the T-163 is to extend the logic driving capabilities of flip-flops.

Level shift caused by the NPN emitter follower input is very nearly compensated by an opposite level shift at the PNP emitter follower output. Delay time, under most applications, is negligible and the output, for all practical purposes, is identical to the input except that it has increased load capabilities. The input impedance is approximately 20 K ohms minimum to −12 volts DC and two T-163 units are permissible loads on each output of flip-flops such as T-101B, T-102A, etc

Each output PNP emitter follower may be treated exactly as a T-111 when considering load-driving ability. Maximum load per T-163 may not exceed that of four T-111 emitter followers. Total logic loading for each T-163 is 12 DC "Or" gates, or 16 DC "And" gates, or 32 DCTL "And" or "Or" gates. Thus, T-163 can be used to extend flip-flop fan-out capabilities to 64 "And" or "Or" loads per output.

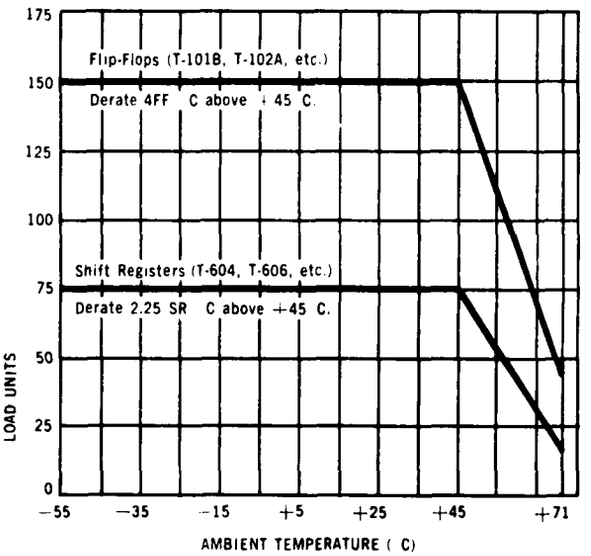
Capacity Driver **T-165** is a transistorized assembly containing three germanium transistors in a pulse amplifier configuration with a low output impedance. The primary purpose of this unit is to drive heavy capacitive loads such as a large number of shift register pulse inputs.

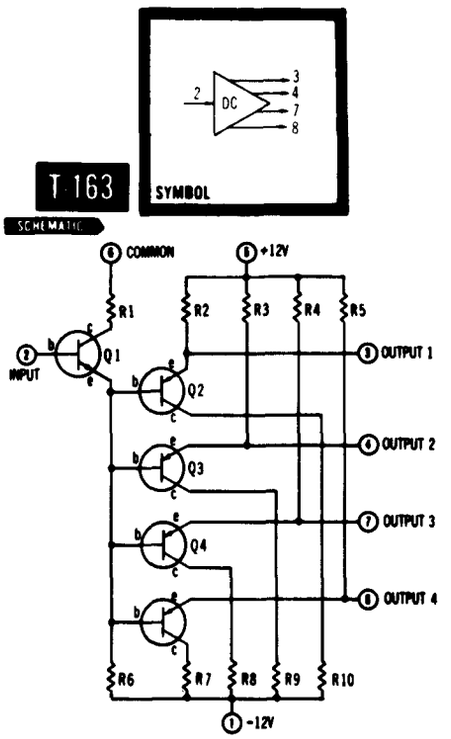
Signal lead length should be as short as possible when driving a large number of units to prevent ringing or overshoot. In addition, signal lead-wire resistance should be kept to a minimum because peak currents as high as 400 ma can be expected when driving the maximum load.

Capacity Driver **T-302** contains a squaring amplifier and a complementary-symmetry emitter-follower output circuit. Anti-saturation techniques are employed to achieve high-frequency response. The primary purpose of this unit is to drive high capacitive loads without appreciable logic level loss or phase shift. DC loading is also permissible.

T-165 — 250Kc LOAD DERATING CHART

(Load can be doubled when frequency is halved within the maximum of 150 Flip-Flops or 75 Shift Registers)





DRIVERS	T-163 D.C. Driver	T-165 Capacity Driver	T-302 Capacity Driver
INPUT			
SIGNAL FREQUENCY RANGE	0 to 250 Kc	0 to 250 Kc	0 to 1 Mc
AMPLITUDE	8V (—11V to —3V shift)	Pulse: 6.5V P-P min.†† 9.0V P-P max.	8V (—11 to —3V shift)
RISE TIME	0.5 to 1.0 μsec	0.5 μsec max.	0.05 to 0.3 μsec
INPUT LOAD CHARACTERISTICS:			
A, B	10, 25	0, 100	50, 500
C, D	5, 25	0, 75	0, 700
E, F	10, 25	0, 100	50, 500
OUTPUT (each output)			
AMPLITUDE	*‡ approx. equal to input amplitude with: max. loss at —3V level = —0.25V max. loss at —11V level = +0.6V	8.0 to 8.3V P-P pulse depending on frequency	—11V to —3V DC level shift
RISE TIME	equal to input rise time	0.4 μsec max. with maximum loads shown on chart•	0.15 μsec max.•
FALL TIME	equal to input fall time	2.0 μsec max. with maximum loads shown on chart•	0.20 μsec max.•
PULSE WIDTH	depends on input	2.5 μsec max. with maximum loads shown on chart	depends on input
DELAY TIME	0.15 μsec max.	0.6 μsec max. with maximum loads shown on chart	0.15 μsec max.
OUTPUT DRIVE CHARACTERISTICS	CD type IV†	C = 1000; D = 10,000	C = 1000; D = 10,000
POWER REQUIRED			
—12 VDC ±10%	24 ma max.	15.7 ma quiescent, 130 ma max. depending on load	33 ma average
+12 VDC ±10%	15 ma max.	2.5 ma max.	none
OPERATING TEMPERATURE RANGE	—55 to +71 C	—55 to +71°C	—55 to +71°C

* **CAUTION:** Outputs may not be paralleled. Each output must be loaded independent of remaining outputs.

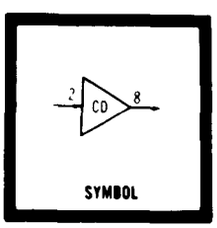
† When operating into a purely capacitive load connect an external 5.6KΩ resistor from output to +12V supply.

‡ Ringing: Under adverse conditions of temperature, supply voltage, and load connections high-frequency ringing may be experienced at the —3V level with amplitudes slightly exceeding 1V P-P. This is **not** detrimental to 250 Kc operations of T-series units but may be compensated for by inserting a 100 Ω resistor in series with each output pin.

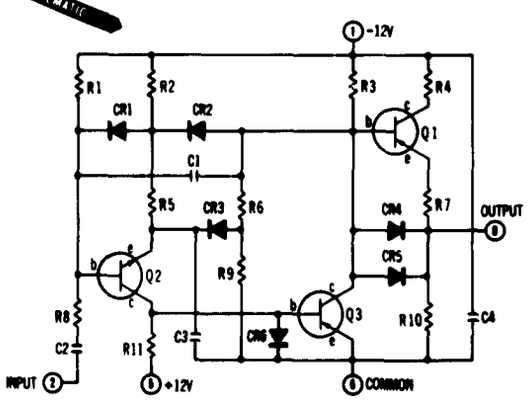
†† Noise Rejection. 1.5V P-P.

• Faster rise and fall times obtainable with lighter loading.

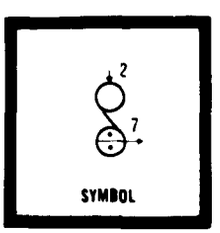
T 165



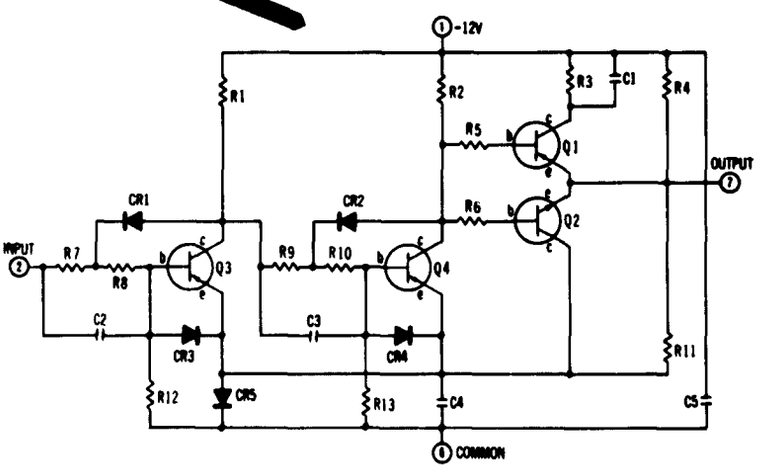
SCHEMATIC



T 302



SCHEMATIC



EMITTER FOLLOWERS T-111, T-112, T-113, T-114, T-115, T-116, T-161, T-652, T-304, T-307

DESCRIPTION

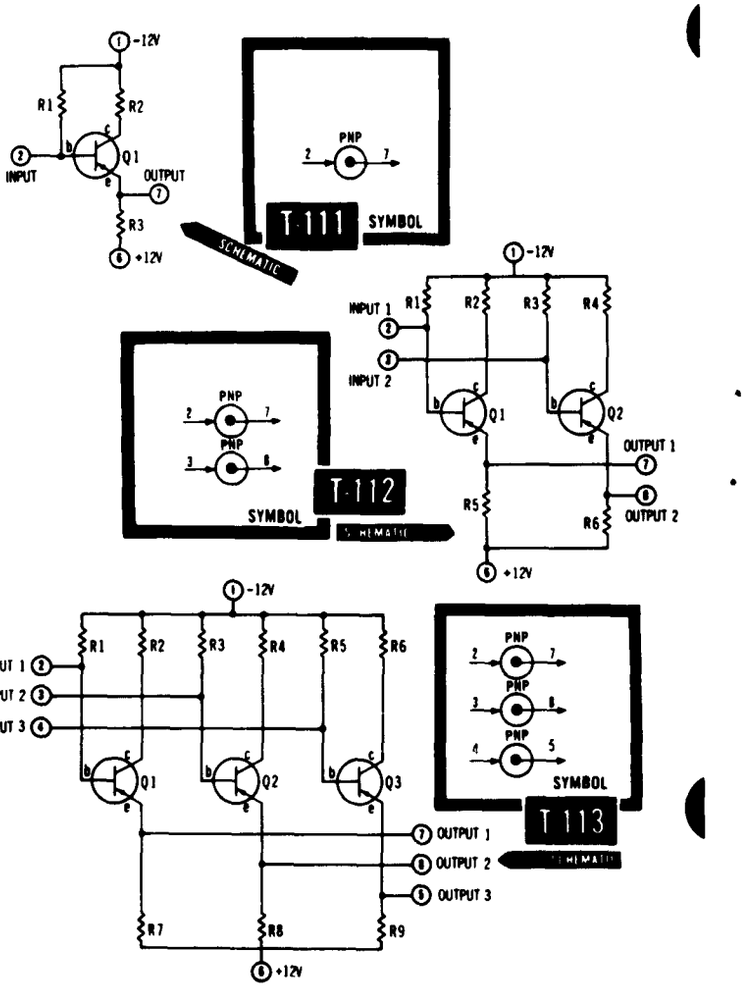
(See "Use of Emitter Followers" in "Family Information" section.)

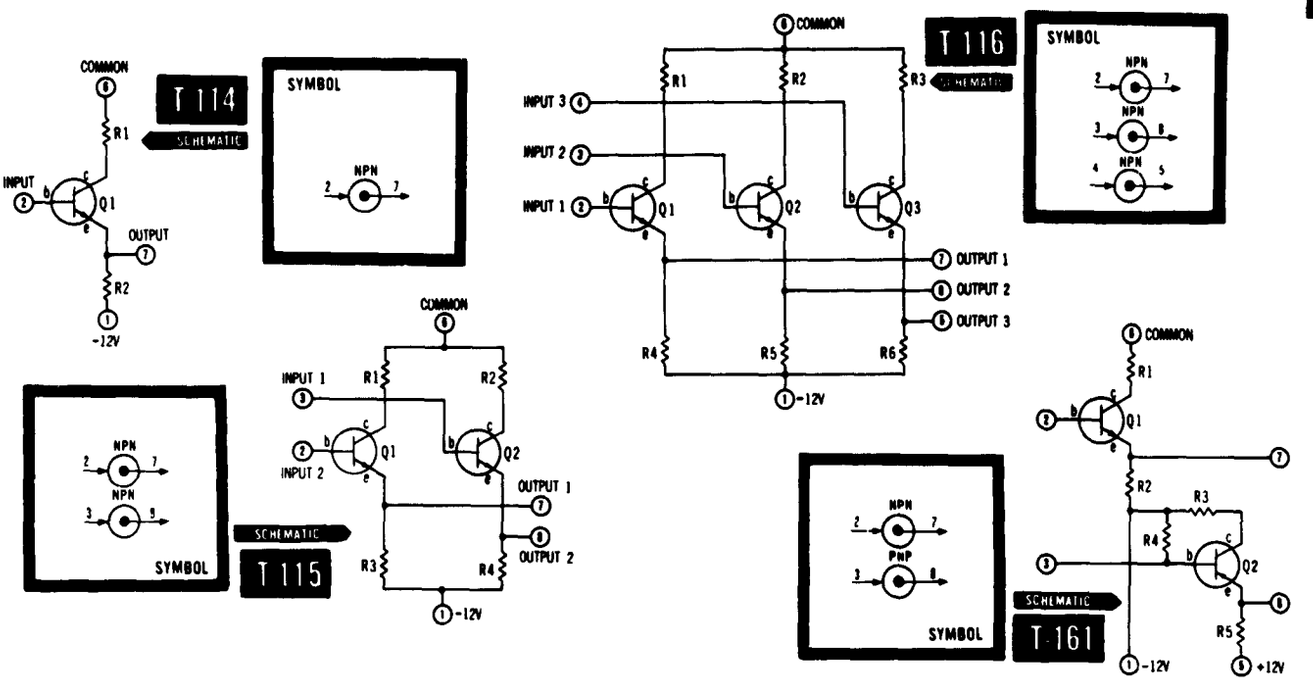
The **T-111, T-112,** and **T-113** are arrangements of the same basic PNP emitter follower in single-, dual-, and triple-circuit packages. PNP emitter followers are used principally to increase load-driving ability into resistive loads such as DC Logic. When necessary to operate into a capacitive load, connect a 5.6KΩ resistor from each output to the +12-volt supply.

The **T-114, T-115,** and **T-116** are arrangements of the same basic NPN emitter follower in single-, dual-, and triple-circuit packages. NPN emitter followers are used principally to increase load-driving ability into capacitive loads such as flip-flops or one-shots. NPN emitter followers are not recommended for operating into DC Logic.

T-161 is a dual package consisting of a PNP emitter follower (T-111) and an NPN emitter follower (T-114) in one container. **T-652** is a dual T-161. These two units can be used to fill odd requirements for emitter followers in a system. Additionally, these units find service as complementary symmetry emitter followers when the inputs are connected together and the outputs are connected together. Since NPN emitter followers have minimum output impedance for positive-going signals and PNP emitter followers have minimum output impedance for negative-going signals, parallel connection of one of each of these types (a complementary symmetry emitter follower) results in a circuit having a very low output impedance for driving capacitive loads.

T-304 and **T-307** are single and dual versions of a complementary symmetry emitter follower for use at frequencies up to 1Mc.





EMITTER FOLLOWERS	PNP Emitter Followers T-111, T-112 (dual), T-113 (triple)	NPN Emitter Followers T-114, T-115 (dual), T-116 (triple)	PNP/NPN Emitter Followers T-161 T-652	Complementary Emitter Followers T-304, T-307 (dual)
INPUT				
SIGNAL FREQUENCY RANGE	0 to 250 Kc*	0 to 250 Kc*	0 to 250 Kc*	0 to 1 Mc
SIGNAL AMPLITUDE: NORMAL	—11 to —3V level shift	—11 to —3V level shift	—11 to —3V level shift	—11 to —3V level shift
Maximum Pulse	12V P-P†	12V P-P†	12V P-P†	12V P-P†
INPUT LOAD CHARACTERISTICS:				
A, B	10, 25	10, 25	10, 25	5, 50
C, D	5, 25	0, 100	Pins 7 & 13 outputs loaded: 0, 100 Pins 8 & 14 outputs loaded: 5, 25	5, 25
E, F	10, 25	10, 25	10, 25	5, 50
OUTPUT				
AMPLITUDE	input signal amplitude	input signal amplitude	input signal amplitude	input signal amplitude with level loss from each extreme as follows:
LEVEL SHIFT	0.25V positive	0.25V negative	PNP: 0.25V positive NPN: 0.25V negative	T-304 = 0.25V T-307 = 0.4V
RISE TIME	★	0.1 μsec max. deterioration from input signal‡	PNP: ★ NPN: See T-114, T-115, T-116	same as input signal
DRIVE CHARACTERISTICS	CD type IV††	EF type VIII	Pins 7, 13: EF type VIII Pins 8, 14: CD type IV††	A = 1000, B = 500
OUTPUT IMPEDANCE:				
Neg.-going signal	150 Ω	1.8 KΩ max.	PNP: 150 Ω NPN: 1.8 KΩ	100 Ω max.
Pos.-going signal	5.6 KΩ max.	150 Ω	PNP: 5.6 KΩ NPN: 150 Ω	100 Ω max.
POWER REQUIRED (each emitter follower)				
—12 VDC ±10%	3.9 to 11 ma depending on load	1 to 7 ma depending on load	T-161: 4.9 to 18 ma depending on load T-652: 9.8 to 36 ma depending on load	T-304: 10 ma max. T-307: 20 ma max.
+12 VDC ±10%	3.9 to 11 ma depending on load	none	T-161: 3.9 to 11 ma depending on load T-652: 7.8 to 22 ma depending on load	none
OPERATING TEMPERATURE RANGE	—45 to +65 C	—54 to +71°C	—45 to +65°C	—55 to +71°C

* Frequency Range extends to 500 Kc with slightly reduced output signal.

† When coupled through a suitable capacitor. The input pin must be biased by a resistor returning to the appropriate bias. This RC network can also be used to convert voltage steps into pulses.

‡ Under maximum capacitive loading, rise-time deterioration will not exceed 0.2 μsec.

†† When operating into pure capacitive load, connect a 5.6 KΩ external resistor from output to +12V supply.

★ For inputs with rise times faster than 0.5 μsec., output is 0.5 μsec. max. For slower input rise time, output rise time equals input rise time.

RST FLIP-FLOPS
T-101B, T-157, T-633, T-643, T-644

DESCRIPTION

T-101B is a general-purpose RST flip-flop for use as a storage or memory device or for frequency division. Saturated operation of the transistors is employed at a sacrifice of higher-speed operation to obtain maximum independence of transistor parameter variations and to provide maximum stability and reliability. T-101B (and all of the other RST flip-flops described here) can be triggered in either of two modes:

(1) In the T (trigger or binary) mode, each input pulse changes the state of the flip-flop.

(2) In the RS (reset and set) mode, the circuits respond to **alternate** set and reset pulses; for example, successive set pulses do not disturb the set state. Direct Reset inputs are for use when several flip-flops are to be reset synchronously by a T-109 Reset Generator.

T-157 is similar to T-101B except the trigger input is buffered by an integral NPN emitter follower to reduce the AC load effect of this circuit **T-633** is admirably suited for use with the Digital Systems Breadboard and Training equipment (described under "Related Equipment") because it contains DC, AC, and direct base connections on both the set and reset sides of the flip flop as well as a trigger input.

T-643 and **T-644** are basically the same as T-101B except T-643 contains integral PNP emitter followers on both outputs and T-644 contains an integral PNP emitter follower on one output. These emitter followers provide considerably increased load-driving ability.

RST FLIP-FLOPS	T-101B	T-157	T-633	T-643	T-644
INPUT					
SIGNAL FREQUENCY RANGE:					
T Mode	0 to 250 Kc†	0 to 250 Kc	0 to 250 Kc†	0 to 250 Kc †	0 to 250 Kc
RS Mode	0 to 250 Kc* ‡	0 to 250 Kc*	0 to 250 Kc* ‡	0 to 300 Kc*	0 to 250 Kc*
AMPLITUDE (except base inputs)					
Maximum	9V P-P	9V P-P	9V P-P	9V P-P	9V P-P
Minimum (pos-going pulse) @ rise time up to 1.0 μsec)▪	6V P-P	6V P-P	6V P-P	6V P-P	6V P-P
AMPLITUDE (base input)	—NA—	—NA—	DC level shift 3.5 to 1.0V	—NA—	—NA—
RISE TIME	0.1 to 1.0 μsec	0.1 to 1.0 μsec	0.1 to 1.0 μsec	0.1 to 1.0 μsec	0.1 to 1.0 μsec
INPUT LOAD CHARACTERISTICS:					
TRIGGER inputs:					
A, B	10, 100	10, 25	10, 100	10, 100	10, 100
C, D	8, 75	0, 100	8, 75	8, 75	8, 75
E, F	10, 100	10, 25	10, 100	10, 100	10, 100
AC SET & RESET inputs:					
A, B	25, 100	25, 100	25, 100	25, 100	25, 100
C, D	20, 75	20, 75	20, 75	20, 75	20, 75
E, F	25, 100	25, 100	25, 100	25, 100	25, 100
DIRECT inputs: (Refer to Description)					
A, B	10, 0	10, 0	Direct: 10, 0 Base: 15, 0	10, 0	10, 0
OUTPUT					
AMPLITUDE (nominal DC levels)	—3V "1", —11V "0"	—3V "1", —11V "0"	—3V "1", —11V "0"	—3V "1", —11V "0"	—3V "1", —11V "0"
RISE TIME (depending on load & input signal)	0.2 to 1.0 μsec	0.2 to 1.0 μsec	0.2 to 1.0 μsec	0.2 to 1.0 μsec	0.2 to 1.0 μsec
FALL TIME	approx. 2.0 μsec	approx. 2.0 μsec	approx. 2.0 μsec	approx. 2.0 μsec	approx. 2.0 μsec
LOAD DRIVE CHARACTERISTICS	††T mode: AB type I RS mode: AB type III	††AB type I	††T mode: AB type I RS mode: AB type III	•CD type IV	•T mode: Pin 7: CD type IV Pin 8: AB type I RS mode: Pin 7: CD type IV Pin 8: AB type III
POWER REQUIRED					
—12 VDC ±10%	5 ma	9 ma	5 ma	12.8 to 27 ma depending on load	8.9 to 16 ma depending on load
+12 VDC ±10%	none	none	none	3.9 to 11 ma depending on load	3.9 to 11 ma depending on load
OPERATING TEMPERATURE RANGE	—45 to +65 C	—45 to +65 C	—45 to +65 C	—45 to +65 C	—45 to +65 C

* With duty cycle of driving signal for frequencies above 150 Kc reduced to allow 5.0 μsec recovery time on each input.

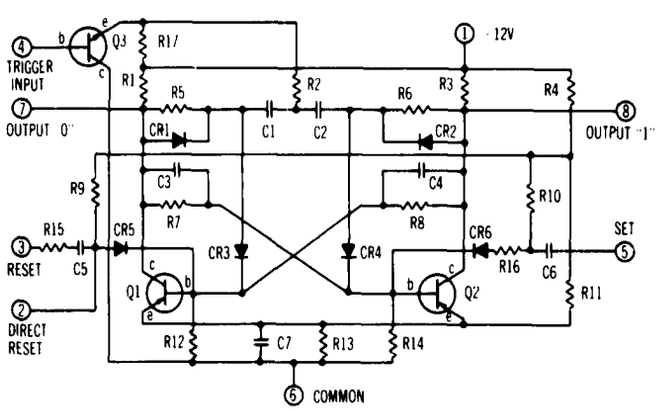
† Range extends to 400 Kc when lightly loaded and with 7V minimum input at 0.4 μsec rise time.

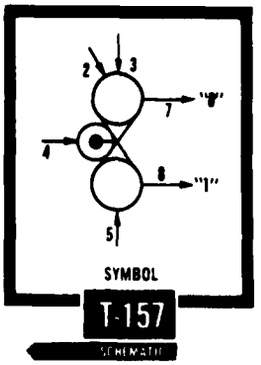
‡ Range extends to 300 Kc with 6.5V minimum input at 1 μsec rise time or faster.

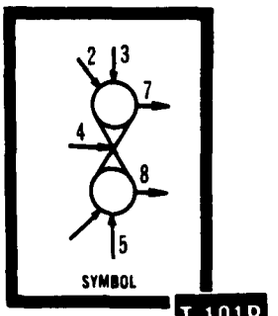
†† Capacitive loading on one output may deteriorate rise time on other output. Rise time can be restored by using emitter follower between flip-flop output and capacitive load.

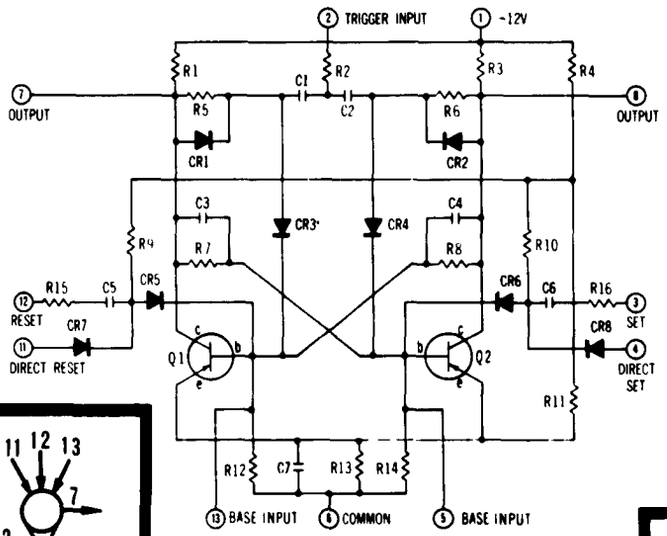
• When operating into capacitive loads, connect a 5.6 KΩ external resistor from output to +12V supply.

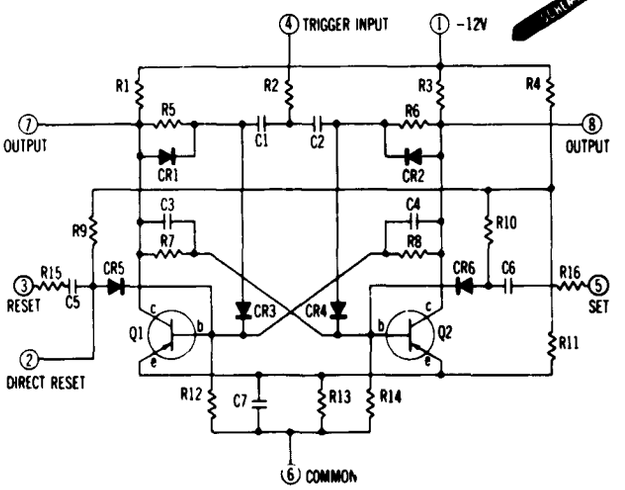
▪ At faster rise times, less amplitude is required. However, these units will not trigger on 1.5V or less regardless of rise time.

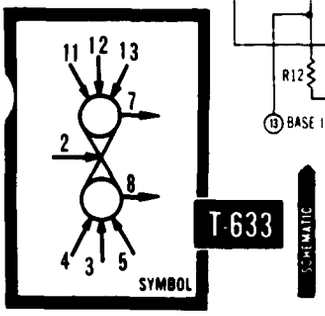

TRIGGER INPUT
OUTPUT "0"
RESET
DIRECT RESET
-12V
OUTPUT "1"
SET
COMMON
Q1
Q2
Q3
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
C1
C2
C3
C4
C5
C6
C7
CR1
CR2
CR3
CR4
CR5
CR6

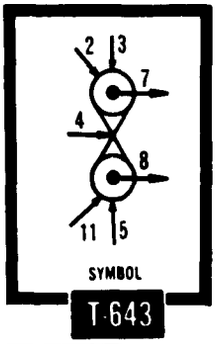

SYMBOL
T-157
SCHEMATIC

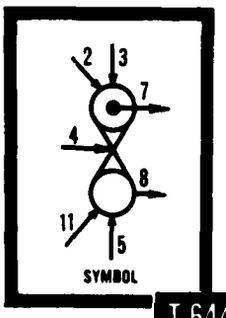

SYMBOL
T-101B
SCHEMATIC

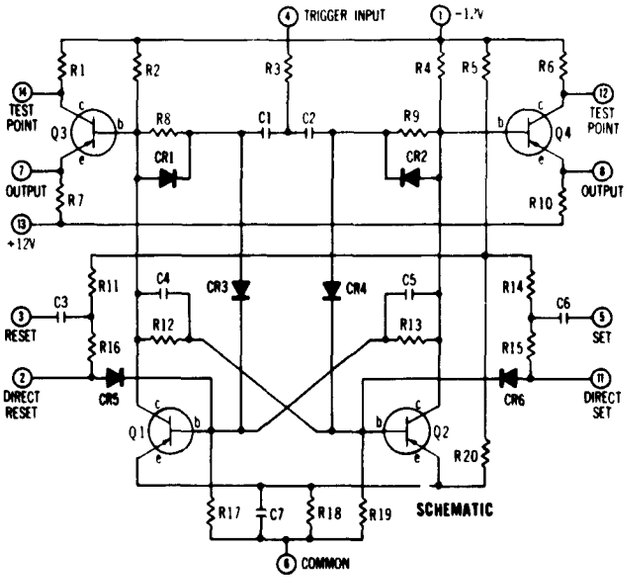

TRIGGER INPUT
-12V
OUTPUT
OUTPUT
RESET
DIRECT RESET
SET
DIRECT SET
BASE INPUT
COMMON
BASE INPUT
Q1
Q2
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
C1
C2
C3
C4
C5
C6
C7
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8

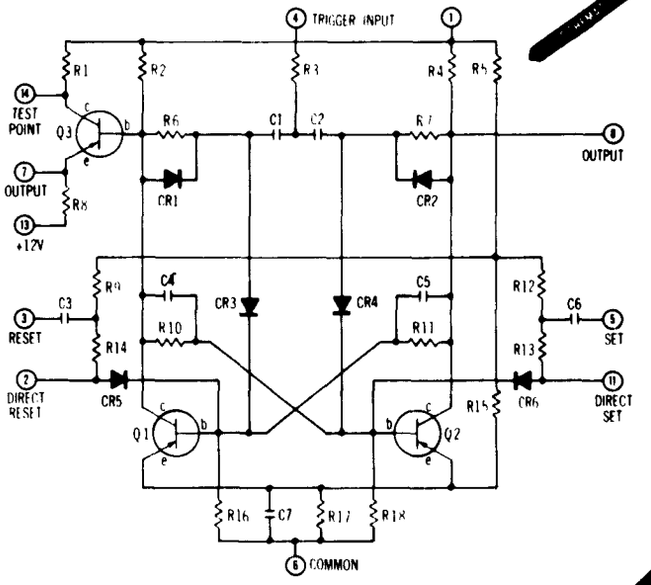

TRIGGER INPUT
-12V
OUTPUT
OUTPUT
RESET
DIRECT RESET
SET
COMMON
Q1
Q2
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
C1
C2
C3
C4
C5
C6
C7
CR1
CR2
CR3
CR4
CR5
CR6


SYMBOL
T-633
SCHEMATIC


SYMBOL
T-643
SCHEMATIC


SYMBOL
T 644
SCHEMATIC


TRIGGER INPUT
-12V
TEST POINT
OUTPUT
+12V
RESET
DIRECT RESET
SET
DIRECT SET
COMMON
SCHEMATIC
Q1
Q2
Q3
Q4
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
C1
C2
C3
C4
C5
C6
C7
CR1
CR2
CR3
CR4
CR5
CR6


TRIGGER INPUT
TEST POINT
OUTPUT
+12V
RESET
DIRECT RESET
SET
DIRECT SET
COMMON
Q1
Q2
Q3
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
C1
C2
C3
C4
C5
C6
C7
CR1
CR2
CR3
CR4
CR5
CR6

T FLIP-FLOPS T-102A, T-303, T-647

DESCRIPTION

T-102A is used as a storage or memory device and as a frequency divider. It is very similar to RST flip-flop T-101B except that the diode-isolated set and reset inputs have been eliminated and replaced with a direct connection to the base of each transistor. This unit is intended, primarily, to be triggered in the T (trigger or binary) mode where each input pulse changes the state of the flip-flop. However, T-102A can be used in set and reset operation where external circuitry permits connections to be made directly to the transistor base. These base connections are normally used in conjunction with Reset Generators T-109 or T-129 (See "Use of Reset Generators" in "Family Information" section of this catalog) but can also be used in conjunction with pulse logic circuits.

T-303 is a T flip-flop for use at frequencies up to 5Mc. An integral emitter follower on the trigger input is provided to increase the input impedance and to produce a more constant input to the flip flop proper regardless of trigger rise time or amplitude. Saturation techniques are used to achieve more uniform transistor operation and, with the transistors used, there is no detraction from operating speeds.

Extreme care should be exercised with external wiring for T-303. In particular, any leads to pins 2 and 3 should be as short as possible and placed away from any leads carrying signals. DC resetting may be done as described in the paragraph "Use of Reset Generators" in the "Family Information" section of this catalog.

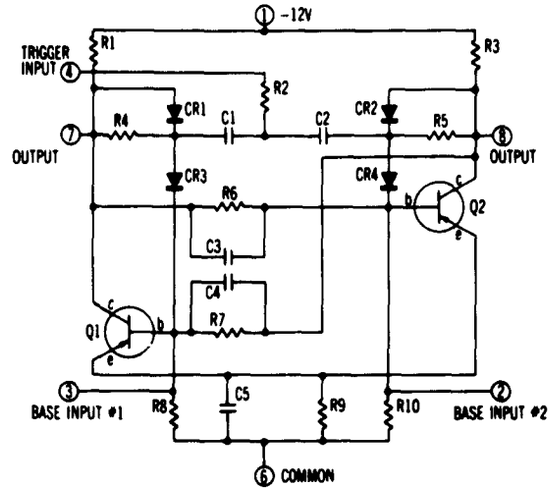
T-647 is a T flip-flop containing integral PNP emitter followers on both outputs to improve DC-load driving ability. Transistor base connections are available for set-reset operation and, additionally, DC set and reset inputs are provided at pins 11 and 5 respectively.

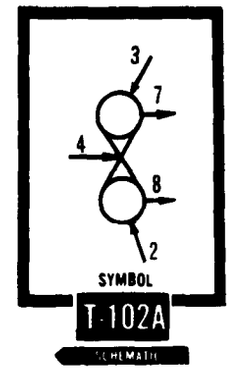
T FLIP-FLOPS	T-102A	T-303	T-647
INPUT			
Trigger Input			
SIGNAL FREQUENCY	0 to 250 Kc	0 to 5 Mc	0 to 250 Kc
AMPLITUDE			
Maximum	9V P-P	9V P-P	9V P-P
Minimum‡	6V pos.-going pulse @ rise times up to 1.0 μsec	6V pos.-going pulse @ rise time up to 0.2 μsec from 0 to 2Mc*	6V pos.-going pulse @ rise time up to 1.0 μsec
RISE TIME	0.1 to 1.0 μsec	0.2 μsec max.*	0.1 to 1.0 μsec
INPUT LOAD CHARACTERISTICS:			
A, B	10, 100	0, 150	10, 100
C, D	8, 75	5, 25	8, 75
E, F	10, 100	0, 150	10, 100
Base Inputs			
MINIMUM AMPLITUDE (DC level shift from:)	—3.5 VDC to —1.0 VDC	0 VDC to —4 VDC	—3.5 VDC to —1.0 VDC
INPUT LOAD CHARACTERISTICS: (Refer to Description)			
A, B	15, 0	30, 0	10, 0
OUTPUT			
AMPLITUDE (nominal DC levels:)	—3V = "1", —11V = "0"	—3V = "1", —11V = "0"	—3V = "1", —11V = "0"
RISE TIME (depending on load, frequency, & input signal)	0.2 to 1.0 μsec	15 to 60 nsec	0.2 to 1.0 μsec
FALL TIME	approx. 2.0 μsec	0.1 to 0.5 μsec	approx. 2.0 μsec
LOAD DRIVE CHARACTERISTICS	AB type I	A:250, B:125	CD type IV†
POWER REQUIRED			
—12 VDC ± 10%	5.0 ma	18.5 ma	4.6 to 27 ma depending on load
+12 VDC ± 10%	none	none	3.9 to 11 ma depending on load
OPERATING TEMPERATURE RANGE	—45 to +65 C	—45 to +65°C	—45 to +65 C

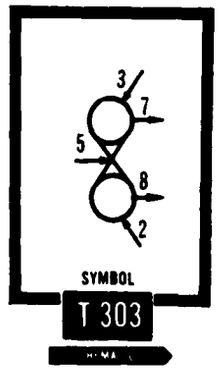
*At 2 to 5 Mc, a rise time of 30% of input period or faster will trigger flip-flop with 6.0V pos.-going wave form. Sine-wave triggering may be extended by increasing input to 6.5V.

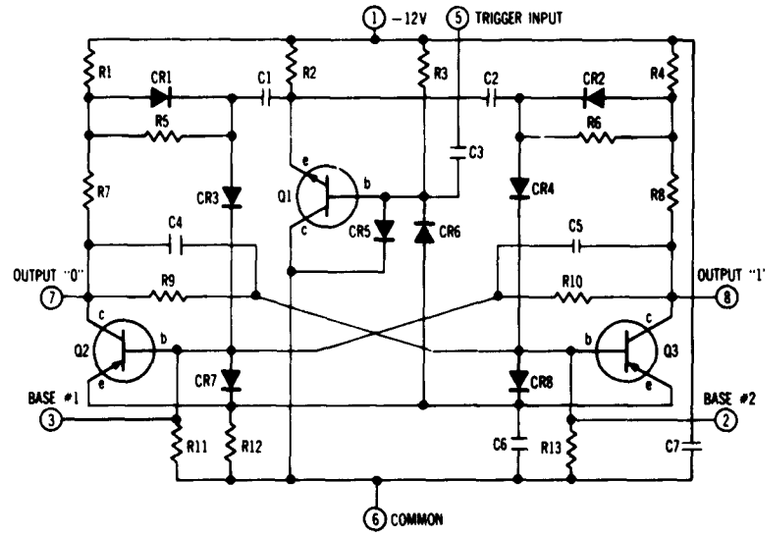
†When operating into capacitive loads, connect external 5.6 KΩ resistor from output to +12V supply.

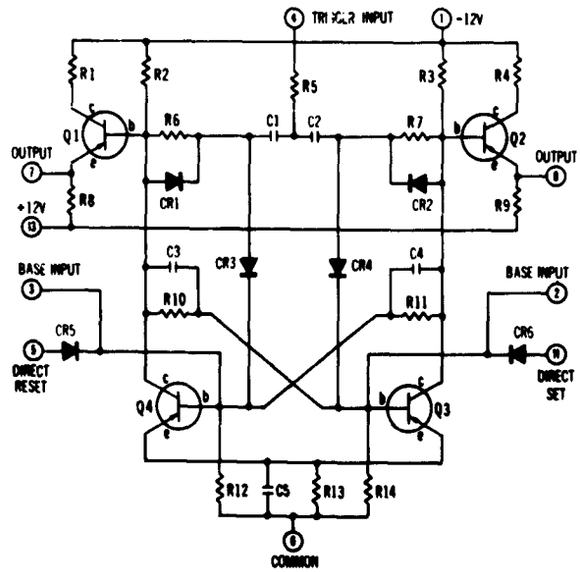
‡At faster rise times, less amplitude is required. However, these units will not trigger on inputs of 1.5V or less regardless of rise time.

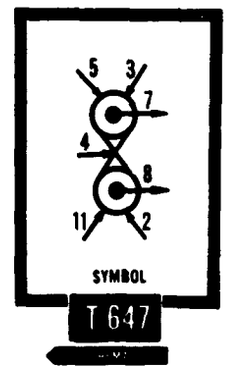

-12V
TRIGGER INPUT
R1
R2
R3
R4
CR1
C1
C2
CR2
R5
OUTPUT
OUTPUT
CR3
R6
CR4
Q2
C3
C4
Q1
R7
BASE INPUT #1
R8
C5
R9
R10
BASE INPUT #2
COMMON


SYMBOL
T-102A


SYMBOL
T 303


-12V
TRIGGER INPUT
R1
CR1
C1
R2
R3
C2
CR2
R4
R5
R6
C3
R7
CR3
Q1
CR4
R8
C4
CR5
CR6
C5
OUTPUT "0"
R9
R10
OUTPUT "1"
Q2
Q3
CR7
CR8
BASE #1
BASE #2
R11
R12
C6
R13
C7
COMMON


TRIGGER INPUT
-12V
R1
R2
R5
R3
R4
Q1
R6
C1
C2
R7
Q2
OUTPUT
OUTPUT
+12V
R8
CR1
CR2
R9
C3
CR3
CR4
C4
BASE INPUT
BASE INPUT
R10
R11
CR5
CR6
DIRECT RESET
DIRECT SET
Q4
Q3
R12
C5
R13
R14
COMMON

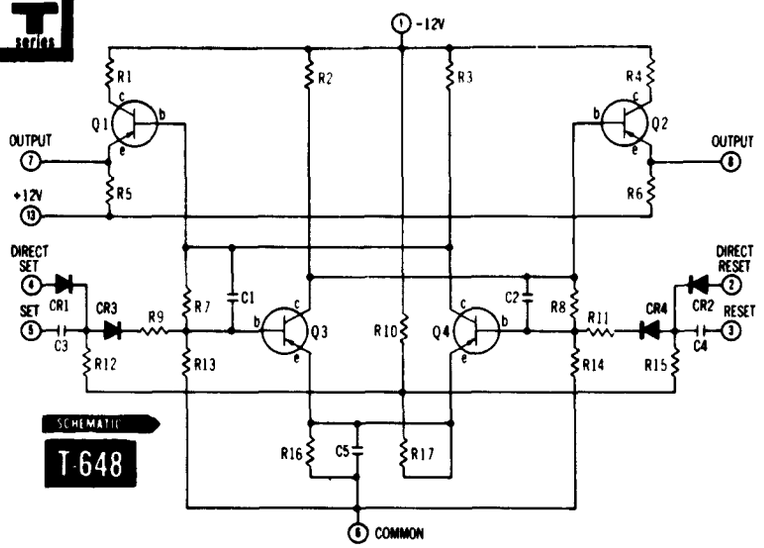

SYMBOL
T 647

RS FLIP-FLOPS T 162, T 646, T 648

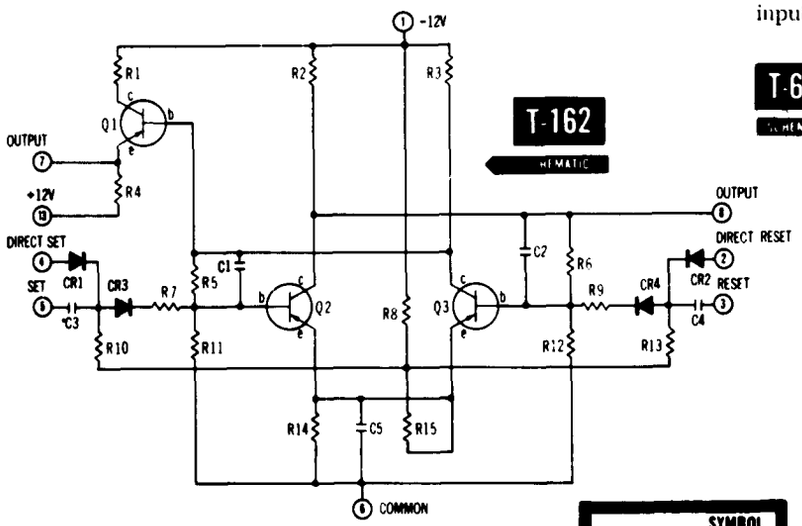
DESCRIPTION

T-162 is an RS flip-flop similar to the general-purpose RST flip-flop T-101B. It differs in that the binary or trigger input has been deleted and a direct set input has been added. **T-646** and **T-648** are similar except T-646 contains an integral PNP emitter follower on one output and T-648 contains integral PNP emitter followers on both outputs. Direct Reset inputs are for use when a number of flip-flops are to be operated in synchronism by a Reset Generator T-109. Isolation diodes on these inputs of T-646 and T-648 prevent feedback when several units are connected together, such as in forming a ring counter. Since T-162 does not contain these diodes, an external isolating diode is necessary whenever both the AC and associated DC inputs are connected.

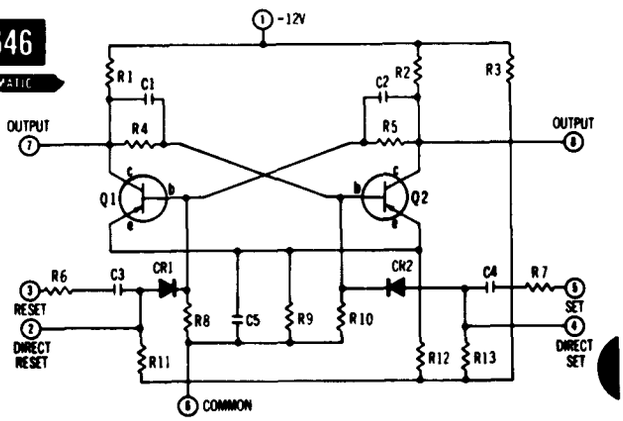
T-648 SCHEMATIC



T-162 SCHEMATIC



T-646 SCHEMATIC



RS FLIP FLOPS	T-162		T-646		T-648	
		SYMBOL		SYMBOL		SYMBOL
INPUT						
SIGNAL FREQUENCY RANGE	0 to 250 Kc*		0 to 300 Kc*		0 to 300 Kc*	
AMPLITUDE:						
Maximum	9V P-P		9V P-P		9V P-P	
Minimum (pos-going pulse @ rise times up to 1 μsec)†	6V P-P		6V P-P		6V P-P	
RISE TIME	0.1 to 1.0 μsec		0.1 to 1.0 μsec		0.1 to 1.0 μsec	
INPUT LOAD CHARACTERISTICS: (Refer to Description)	Pins 3 & 5 (AC)	Pin 2 (direct)	Pins 3 & 5 (AC)	Pin 2 (direct)	Pins 3 & 5 (AC)	Pins 2 & 4 (direct)
A, B	25, 100	10, 0	35, 200	15, 0	35, 200	15, 0
C, D	20, 75	NA	30, 150	NA	30, 150	NA
E, F	25, 100	NA	35, 200	NA	35, 200	NA
OUTPUT						
AMPLITUDE (nominal DC levels)	—3V = "1", —11V = "0"		—3V = "1", —11V = "0"		—3V = "1", —11V = "0"	
RISE TIME (depending on load & input signal)	0.2 to 1.0 μsec		0.4 to 1.0 μsec		0.4 to 1.0 μsec	
FALL TIME (depending on load & input signal)	approx. 2.0 μsec		approx. 1.5 μsec		approx. 1.5 μsec	
LOAD DRIVE CHARACTERISTICS	AB type III		Pin 7: CD type IV†† Pin 8: AB type II‡		CD type IV††	
POWER REQUIRED						
—12 VDC ±10%	5 ma		8.9 to 16 ma depending on load		8.9 to 27 ma depending on load	
+12 VDC ±10%	none		3.9 to 11 ma depending on load		3.9 to 11 ma depending on load	
OPERATING TEMPERATURE RANGE	—45 to +65°C		—45 to +65°C		—45 to +65°C	

* With duty cycle of driving signal for frequencies above 150 Kc reduced to allow 5 μsec recovery time on each input.

† At faster rise times, less amplitude is required. However, these units will not trigger on inputs of 1.5V or less regardless of rise itme.

‡ Capacitive loading on pin 8 may deteriorate rise time of pin 7 output. Output rise time can be restored by using emitter follower between flip-flop output and capacitive load.

†† When operating into capacitive loads, connect external 5.6 KΩ resistor from output to +12V supply.

SHIFT REGISTER and GATED FLIP-FLOPS
T-301A, T-604, T-605, T-606, T-610, T-629, T-801A

DESCRIPTION

T-301A and **T-801A** are gated high-frequency flip-flops connected in Eccles-Jordan type bistable circuits. Anti-saturation techniques are employed to achieve high-frequency response. One of two input gates is enabled by a DC voltage level and the flip-flop is triggered by pulses supplied at a common input. A "DC Reset" is provided for use when a number of flip-flops are to be synchronously reset by a DC Reset Generator T-109. T-801A also has AC-coupled "Reset" and "Set" inputs along with a direct base input to provide maximum versatility.

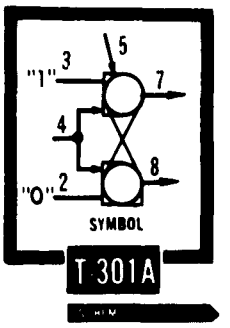
T-604 and **T-629** are gated flip-flops for use where a flip-flop with gated set and reset inputs is required. These units also have provisions for parallel entry of binary "1"'s. The load characteristics for the parallel-data input lines and the "transfer data" inputs are identical to those called out for Data inputs and Shift Pulse inputs respectively in the specification table. T-629 has a Direct Reset input and T-604 has a direct base input connection which can be used to either set or reset the flip-flop. Both of these units have an additional ungated trigger input f special operations.

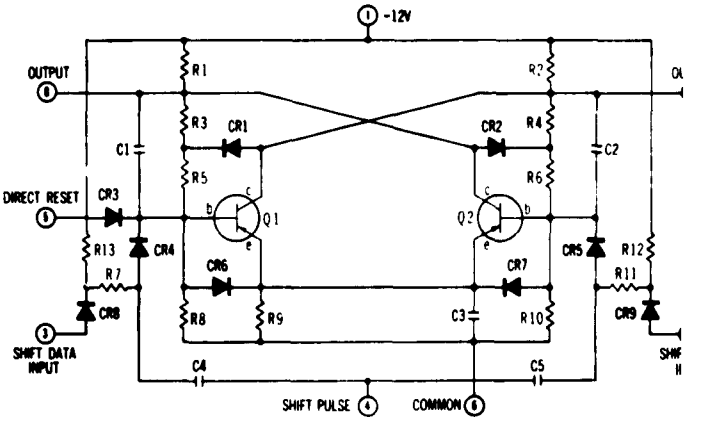
T-605, T-606 and **T-610** are complete shift elements, co taining the storage and gating circuits within a sing package. One of the models, T-606, is a general-purpo element for flexible application. The T-605 and T-6 units each include an output emitter follower to facilit parallel loading into DC logic.

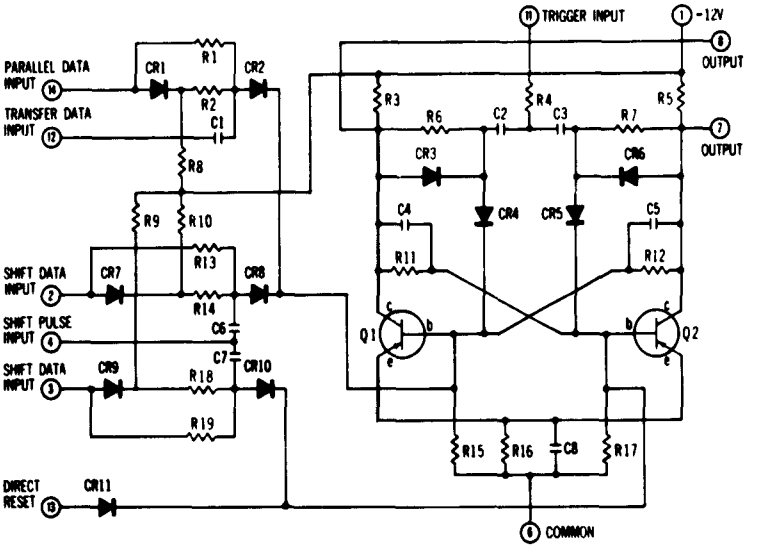
The usual areas of application for these circuits are:

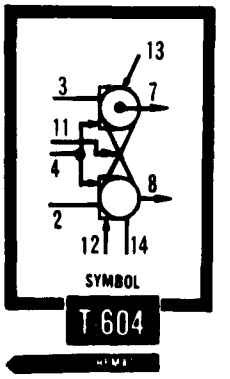
T-605 — Parallel-in, parallel-out.
T-606 — Serial-in, serial-out; or parallel-in- serial-out.
T-610 — Serial-in, parallel-out.

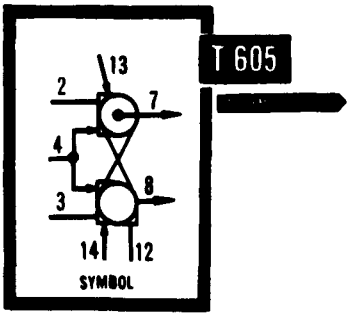
The T-605 is a slow-speed element that will work at spee up to 25Kc. The T-606 and T-610 are both medium-spe devices that will work at speeds up to 250Kc.

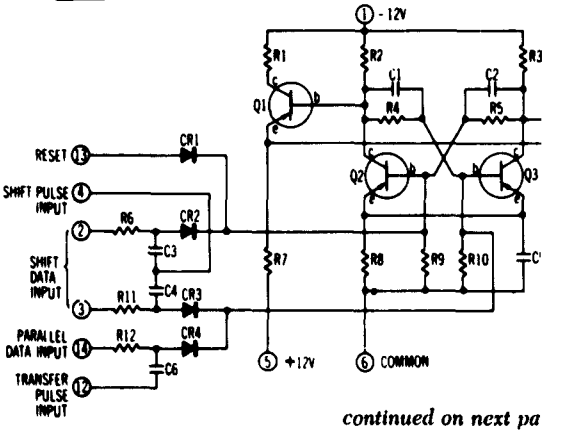












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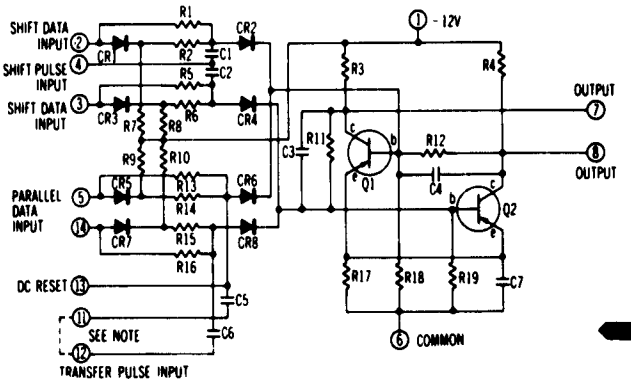
SHIFT REGISTER and GATED FLIP-FLOPS	T-301A Gated F/F (1 Mc)	T-604 Gated F/F (250 Kc)	T-605 Shift Reg. F/F (25 Kc)	T-606 Shift Reg. F/F (250 Kc)	T-610 Shift Reg. F/F (250 Kc)	T-629 Gated F/F (250 Kc)	T-801A Gated F/F (1 Mc)
INPUT							
Data Input							
SIGNAL FREQUENCY RANGE	0 to 500 Kc	0 to 125 Kc	0 to 12.5 Kc	0 to 125 Kc	0 to 125 Kc	0 to 125 Kc	0 to 500 Kc
SIGNAL LEVEL (nominal)							
Enable	—2.5 to —4.0 VDC	—3 VDC	—3 VDC	—3 VDC	—3 VDC	—3 VDC	—2.5 to —4.0 VDC
Disable	—10 to —12 VDC	—11 VDC	—11 VDC	—11 VDC	—11 VDC	—11 VDC	—10 to —12 VDC
RISE TIME (μsec)	0.05 to 0.5	0.1 to 1.0	0.1 to 1.0	0.1 to 1.0	0.1 to 1.0	0.1 to 1.0	0.05 to 0.3
INPUT LOAD CHARACTERISTICS:							
A, B	5, 150	10, 25	65, 200	10, 25	10, 25	10, 25	5, 150
C, D	5, 50	10, 50	5, 25	10, 50	10, 50	10, 50	5, 50
E, F	5, 150	10, 25	65, 200	10, 25	10, 25	10, 25	5, 150
Shift Pulse							
SIGNAL FREQUENCY RANGE	0 to 1 Mc	0 to 250 Kc	0 to 25 Kc	0 to 250 Kc	0 to 250 Kc	0 to 250 Kc	0 to 1 Mc
AMPLITUDE							
Maximum	9V P-P	9V P-P	9V P-P	9V P-P	9V P-P	9V P-P	9V P-P
Minimum	6V P-P	7.5V P-P	6V P-P	7.5V P-P	7.5V P-P	7.5V P-P	6V P-P
RISE TIME (μsec)	0.05 to 0.2	0.4 (max.)	0.1 to 1.0	0.4 (max.)	0.4 (max.)	0.4 (max.)	0.05 to 0.2
INPUT LOAD CHARACTERISTICS:							
A, B	10, 100	25, 200	10, 150	25, 200	25, 200	25, 200	10, 100 •
C, D	8, 75	20, 150	8, 115	20, 150	20, 150	20, 150	8, 75 •
E, F	10, 100	25, 200	10, 150	25, 200	25, 200	25, 200	10, 100 •
Ungated Trigger							
SIGNAL FREQUENCY RANGE	— NA —	0 to 250 Kc	— NA —	— NA —	—NA —	0 to 250 Kc	— NA —
AMPLITUDE							
Maximum	— NA —	9V P-P	— NA —	— NA —	—NA —	9V P-P	— NA —
Minimum (pos.-going pulse @ rise times up to 1 μsec)*	— NA —	6V P-P	— NA —	— NA —	—NA —	6V P-P	— NA —
RISE TIME (μsec)	— NA —	0.1 to 1.0	— NA —	— NA —	— NA —	0.1 to 1.0	—NA —
INPUT LOAD CHARACTERISTICS:							
A, B	— NA —	10, 100	— NA —	— NA —	—NA —	10, 100	— NA —
C, D	— NA —	8, 75	— NA —	— NA —	—NA —	8, 75	— NA —
E, F	— NA —	10, 100	— NA —	—NA —	— NA —	10, 100	— NA —
Direct Reset							
REQUIRES SAME OUTPUT AS THAT GENERATED BY	T-109	T-109‡	T-109	T-109†	T-109	T-109	T-109
INPUT LOAD CHARACTERISTICS: (Refer to Description)	30, 0	15, 0	10, 0	15, 0	10, 0	10, 0	30, 0
OUTPUT							
AMPLITUDE (Nominal DC levels)	—3V = "1", —11V = "0"	—3V = "1", —11V = "0"	—3V = "1", —11V = "0"	—3V = "1", —11V = "0"	—3V = "1", —11V = "0"	—3V = "1", —11V = "0"	—3V = "1", —11V = "0"
RISE TIME (in μsec & depending on load and input signal)	0.05 to 0.2	0.2 to 1.0	0.2 to 1.0	0.2 to 1.0	0.2 to 1.0	0.2 to 1.0	0.05 to 0.2
FALL TIME (in μsec)	0.5 (max.)	2.0 (approx.)	2.0 (approx.)	2.0 (approx.)	2.0 (approx.)	2.0 (approx.)	0.5 (max.)
LOAD DRIVE CHARACTERISTICS:	AB type VI	Trigger Mode: AB type I SR Mode: AB type V	Pin 7: CD type IV Pin 8: AB type V	AB type V	Pin 7: CD type IV Pin 8: AB type V	Trigger Mode: AB type I SR Mode: AB type V	AB type VI
POWER REQUIRED							
—12 VDC ±10%	11 ma	7.3 ma	8.9 to 16 ma	6.6 ma max.	9.8 to 16.9 ma	7.3 ma max.	11 ma
+12 VDC ±10%	none	none	3.9 to 11 ma	none	3.9 to 11 ma	none	none
OPERATING TEMPERATURE RANGE	—45 to +65°C	—45 to +65°C	—45 to +65°C	—45 to +65°C	—45 to +65°C	—45 to +65°C	—45 to +65°C

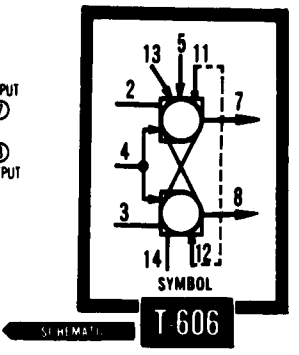
* At faster rise times, less amplitude is required. However, these units will not trigger on 1.5V or less regardless of rise time.

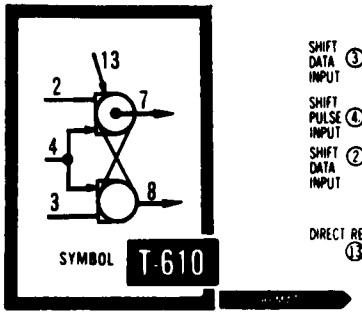
† Connect external resistor from Pin 13 to 12V common. Value = $\frac{10{,}000}{N}$ where N is the number of Shift Register elements.

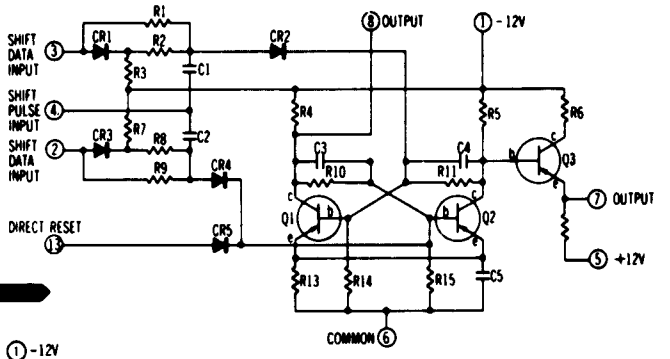
‡ Connect external diode to isolate transistor base circuit from T-109 output circuit.

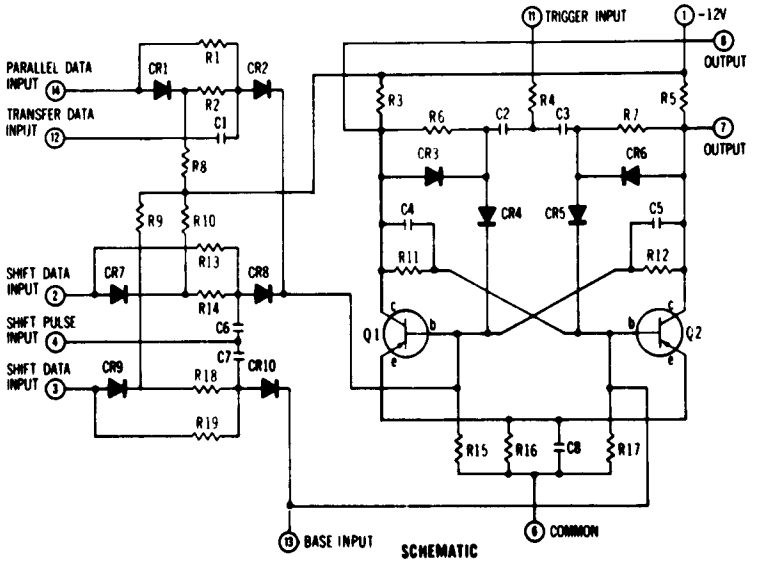
• Pins 4, 12 and 13.

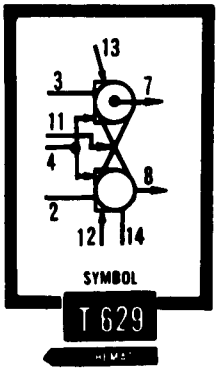

SHIFT DATA INPUT
SHIFT PULSE INPUT
SHIFT DATA INPUT
PARALLEL DATA INPUT
DC RESET
SEE NOTE
TRANSFER PULSE INPUT
-12V
OUTPUT
OUTPUT
COMMON

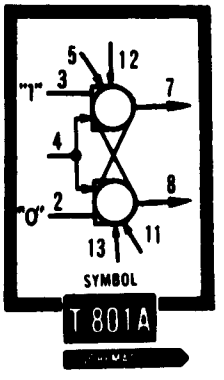

SYMBOL
T-606

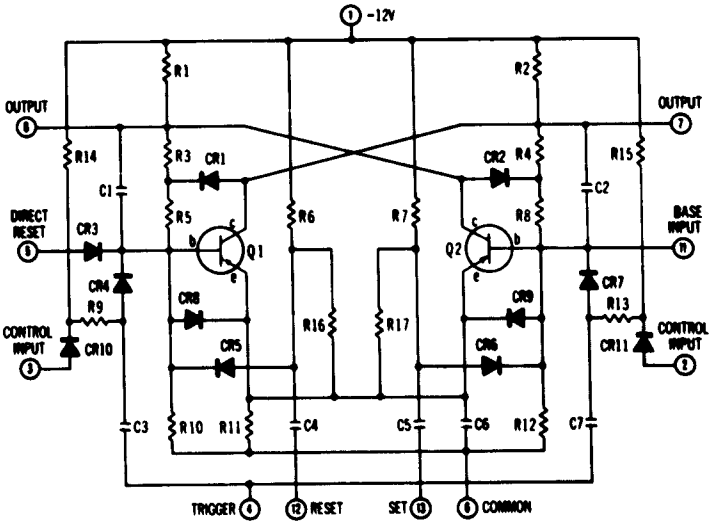

SYMBOL
T-610


SHIFT DATA INPUT
SHIFT PULSE INPUT
SHIFT DATA INPUT
DIRECT RESET
OUTPUT
-12V
OUTPUT
+12V
COMMON


PARALLEL DATA INPUT
TRANSFER DATA INPUT
SHIFT DATA INPUT
SHIFT PULSE INPUT
SHIFT DATA INPUT
TRIGGER INPUT
-12V
OUTPUT
OUTPUT
BASE INPUT
COMMON
SCHEMATIC


SYMBOL
T 629


"1"
"0"
SYMBOL
T 801A


-12V
OUTPUT
OUTPUT
DIRECT RESET
CONTROL INPUT
BASE INPUT
CONTROL INPUT
TRIGGER
RESET
SET
COMMON

INVERTERS T-117, T-136, T-137, T-138

DESCRIPTION

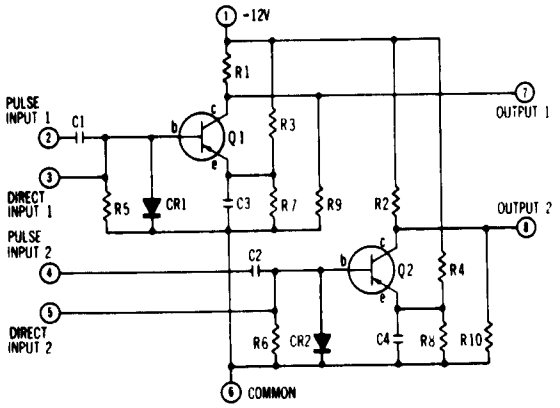
T-117 contains two identical, independent Pulse Inverting Amplifiers. Each amplifier produces a standard positive-going pulse of 1 to 2 microseconds duration for each **negative-going** input pulse or voltage step. Inputs are shaped to produce outputs of improved rise time and standard amplitude.

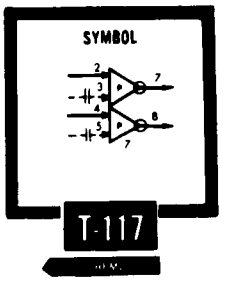
T-136, T-137, and **T-138** are DC inverters or "Not" circuits which are used to provide logic inversion with level restoration. T-136 and T-138 are dual units and one output of T-138 is emitter-follower buffered to provide greater drive capability. T-137 is a single unit with built-in emitter-follower buffering. One note of caution when using T-136: Note that there is no DC return to ground on the output and, consequently, this output can rise to −12V. To establish a −11V output, connect an external 11KΩ resistor from the output pin to ground.

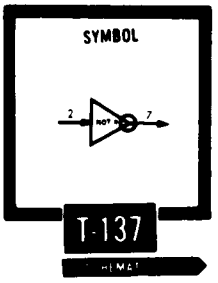
INVERTERS	T-117 Dual Pulse Inverter	T-136 Dual Inverter	T-137 Buffered Inverter	T-138 Dual Inverter
INPUT (each inverter)				
SIGNAL FREQUENCY RANGE	250 Kc max	0 to 250 Kc	0 to 250 Kc	0 to 250 Kc
AMPLITUDE	Min. pulse or step of 6V @ 1 μsec rise time.* Will not respond to 1.5V or less, regardless of rise time	−3V = "1", −11V = "0"	−3V = "1", −11V = "0"	−3V = "1", −11V = "0"
ON CURRENT (Max.)	—NA—	1.02 ma	0.36 ma	Pin 2: 1.02 ma Pin 3: 0.4 ma
OFF CURRENT (Max.)	—NA—	0.4 ma	0.1 ma	Pin 2: 0.4 ma Pin 3: 0.1 ma
RISE TIME	—NA—	0.1 to 1.0 μsec	0.1 to 1.0 μsec	0.1 to 1.0 μsec
FALL TIME	0.1 to 1.0 μsec*	0.1 to 2.0 μsec	0.1 to 2.0 μsec	0.1 to 2.0 μsec
INPUT LOAD CHARACTERISTICS:				
A, B	15, 100	65, 200	40, 100	Pin 2: 65, 200 Pin 3: 40, 100
C, D	50, 75	5, 25	5, 25	5, 25
E, F	15, 100	65, 200	40, 100	Pin 2: 65, 200 Pin 3: 40, 100
OUTPUT (each inverter)				
POLARITY	positive	inverted from input	inverted from input	inverted from input
AMPLITUDE	Leading edge: 9.5V max. 7V min. Trailing edge: 9V max., 7V min.	−3V = "1", −11V = "0"	−3V = "1", −11V = "0"	−3V = "1", −11V = "0"
PULSE WIDTH (half amplitude points)	1.5 to 4.5 μsec depending on input fall time and amplitude	depends on input	depends on input	depends on input
RISE AND FALL TIMES	0.15 to 0.5 μsec	1.0 μsec max.†	1.0 μsec max.†	1.0 μsec max.†
LOAD DRIVE CHARACTERISTICS	AB type VII	AB type XVIII	CD type IV	Pin 7: AB type XVIII Pin 8: CD type IV
POWER REQUIRED				
−12 VDC ±10%	3.0 ma quiescent, 4.5 ma peak	10 ma max.	6.5 ma max.	16.3 ma max.
+12 VDC ±10%	none	1 ma max.	4.0 ma max.	4.4 ma max.
OPERATING TEMPERATURE RANGE	−45 to +65 C	−55 to +71°C	−55 to +71 C	−55 to +71°C

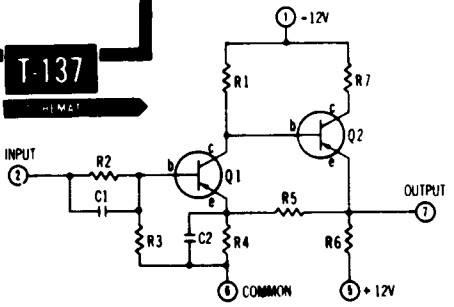
* For signals of very poor rise time use direct input with external capacitor of suitable size.

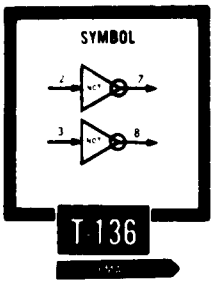
† Faster rise and fall times obtainable with lighter loads.

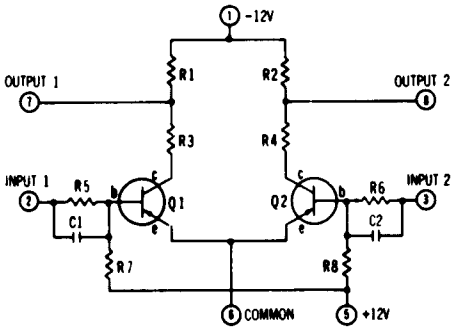

-12V
R1
PULSE INPUT 1
C1
Q1
R3
OUTPUT 1
DIRECT INPUT 1
R5
CR1
C3
R7
R9
R2
OUTPUT 2
PULSE INPUT 2
C2
Q2
R4
DIRECT INPUT 2
R6
CR2
C4
R8
R10
COMMON

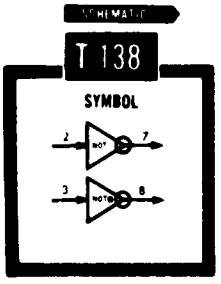

SYMBOL
T-117

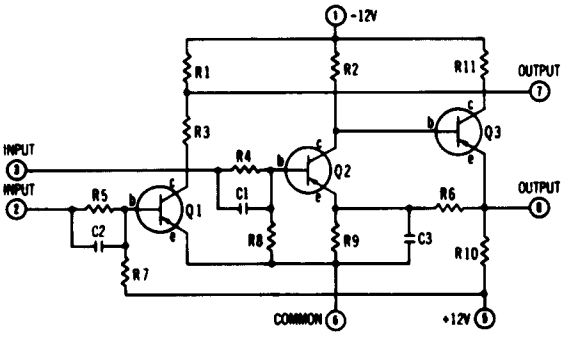

SYMBOL
T-137


-12V
R1
R7
Q2
INPUT
R2
Q1
C1
R5
OUTPUT
R3
C2
R4
R6
COMMON
+12V


SYMBOL
T-136


-12V
OUTPUT 1
R1
R2
OUTPUT 2
R3
R4
INPUT 1
R5
Q1
Q2
R6
INPUT 2
C1
C2
R7
R8
COMMON
+12V


T 138
SYMBOL


-12V
R1
R2
R11
OUTPUT
R3
Q3
INPUT
R4
Q2
INPUT
R5
Q1
C1
R6
OUTPUT
C2
R8
R9
C3
R10
R7
COMMON
+12V

DESCRIPTION

DCTL Logic Gates use transistors connected as emitter followers at each input and all transistors share a common load resistor. The transistor base-emitter circuit functions as a diode and the emitter-follower configuration provides substantial current gain. The relatively high input impedance makes these units relatively light loads on the driving source. Another advantage of these circuits is that no interstage coupling element is required between gates or between gates and amplifiers.

"And" GATES T-309, T-439, T-641, T-650, T-802

The **DCTL "And" Gates** use PNP transistors and operate best into resistive loads. When it is necessary to drive a capacitive load, connect a 5.6KΩ resistor from the output of each gate to the +12-volt supply. This will increase driving ability for positive pulses as described in the "Use of Emitter Follower" paragraph in the "Family Information" section of this catalog.

DCTL "And" GATES	T-309 3-Input	T-439 3-Input	T-641 Dual 2-/single 4-Input	T-650 Dual 3-/single 6-Input	T-802 Dual 2-/single 4-Input
INPUT (Connect unused inputs to —3V)					
SIGNAL FREQUENCY RANGE	0 to 1 Mc	0 to 250 Kc*	0 to 250 Kc*	0 to 250 Kc*	0 to 1 Mc
AMPLITUDE	—11V = "0", —3V = "1"	—11V = "0", —3V = "1"	—11V = "0", —3V = "1"	—11V = "0", —3V = "1"	—11V = "0", —3V = "1"
RISE TIME	0.05 to 0.2 μsec	0.1 to 1.0 μsec	0.1 to 1.0 μsec	0.1 to 1.0 μsec	0.05 to 0.2 μsec
INPUT LOAD CHARACTERISTICS:					
A, B	10, 0	10, 0	10, 0	10, 0	10, 0
C, D	8, 0	8, 0	8, 0	8, 0	8, 0
E, F	10, 0	10, 0	10, 0	10, 0	10, 0
OUTPUT					
AMPLITUDE (equal to:)	input signal	input signal	input signal	input signal	input signal
LEVEL SHIFT	approx. ± 0.4V	approx. +0.3V	approx. +0.3V	approx. +0.3V	approx. +0.4V
RISE TIME:					
Unloaded (approx.)	input rise time	★	★	★	input rise time
Degradation Under Load	0.3 μsec max.	0.2 μsec max.	0.2 μsec max.	0.2 μsec max.	0.3 μsec max.
OUTPUT DRIVE CHARACTERISTICS	CD type IV	CD type IV	CD type IV	CD type IV	CD type IV
POWER REQUIRED (each gate)					
—12 VDC ± 10% (Depending on load)	3.9 to 11 ma	3.9 to 11 ma	3.9 to 11 ma	3.9 to 11 ma	3.9 to 11 ma
+12VDC ± 10% (Depending on load)	3.9 to 11 ma	3.9 to 11 ma	3.9 to 11 ma	3.9 to 11 ma	3.9 to 11 ma
OPERATING TEMPERATURE RANGE	—54 to +71 C	—54 to +71°C	—54 to +71 C	—54 to +71°C	—54 to +71°C

* Can be extended to 500 Kc with reduced load.

★ For inputs with rise times faster than 0.5 μsec., output rise time is 0.5 μsec. max. For slower input rise times, output rise time equals input rise time.

DCTL "Or" GATES	T-310 3-Input	T-440 3-Input	T-642 Dual 2-/single 4-Input	T-651 Dual 3-/single 6-Input	T-803 Dual 2-/single 4-Input
INPUT (Connect unused inputs to —12V)					
SIGNAL FREQUENCY RANGE	0 to 1 Mc	0 to 250 Kc*	0 to 250 Kc*	0 to 250 Kc*	0 to 1 Mc
AMPLITUDE	—11V = "0", —3V = "1"	—11V = "0", —3V = "1"	—11V = "0", —3V = "1"	—11V = "0", —3V = "1"	—11V = "0", —3V = "1"
RISE TIME	0.05 to 0.2 μsec	0.1 to 1.0 μsec	0.1 to 1.0 μsec	0.1 to 1.0 μsec	0.05 to 0.2 μsec
INPUT LOAD CHARACTERISTICS:					
A, B	10, 25	10, 25	10, 25	10, 25	10, 25
C, D	5, 25	5, 25	5, 25	5, 25	5, 25
E, F	10, 25	10, 25	10, 25	10, 25	10, 25
OUTPUT					
AMPLITUDE (equal to:)	input signal	input signal	input signal	input signal	input signal
LEVEL SHIFT	—0.5V max.	approx. —0.25V	approx. —0.25V	approx. —0.25V	—0.5V max.
RISE TIME (equal to:)	input rise time	input rise time	input rise time	input rise time	input rise time
OUTPUT DRIVE CHARACTERISTICS	EF type VIII	EF type VIII	EF type VIII	EF type VIII	EF type VIII
POWER REQUIRED (each gate)					
—12 VDC ± 10% (Depending on load)	1 to 21 ma	1 to 7 ma	1 to 7 ma	1 to 7 ma	1 to 21 ma
OPERATING TEMPERATURE RANGE	—54 to +71 C	—54 to +71°C	—54 to +71 C	—54 to +71°C	—54 to +71°C

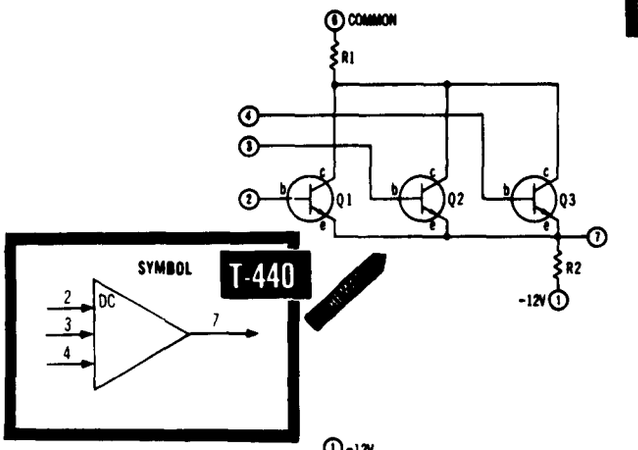
*Can be extended to 500 Kc wth reduced load.

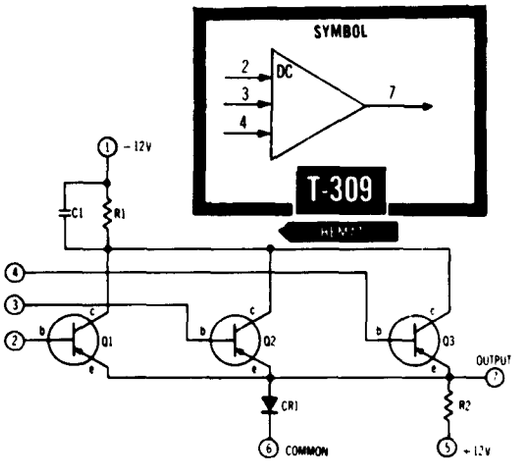
"Or" GATES T-310, T-440, T-642, T-651, T-803

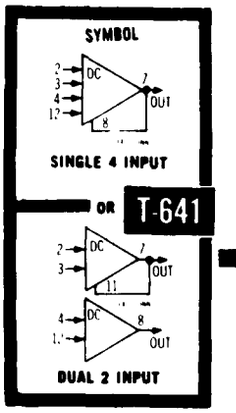
Typical applications for **DCTL "Or" Gates** involve driving capacitive loads such as flip-flops or one-shots. Unused inputs should be connected to the −12-volt supply.

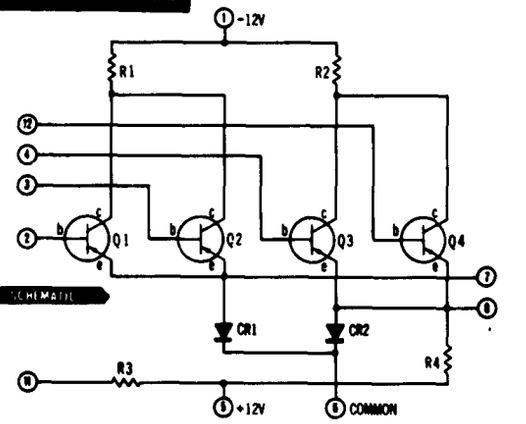
Gates T-641, T-642, T-650, T-651, T-802, and T-803 are exceptionally versatile in that connection of an external jumper determines whether these will be dual gates or single gates. For example, if pins 7 and 8 of T-651 are jumpered, the unit functions as a single 6-input gate; if pins 14 and 8 of T-651 are jumpered, the unit functions as two 3-input gates.

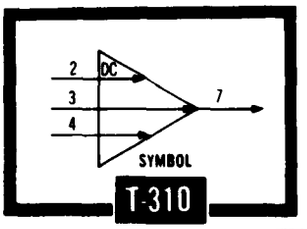
Specifications for one additional DCTL gate, T-653, will be found on the page which contains information describing "And, Or" gates.

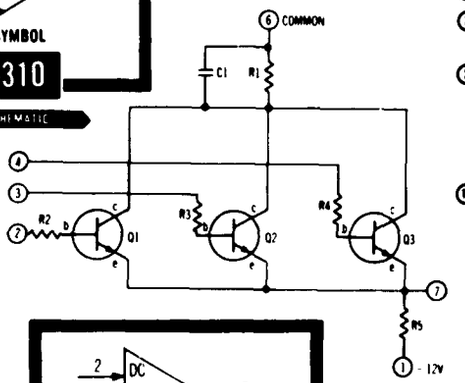


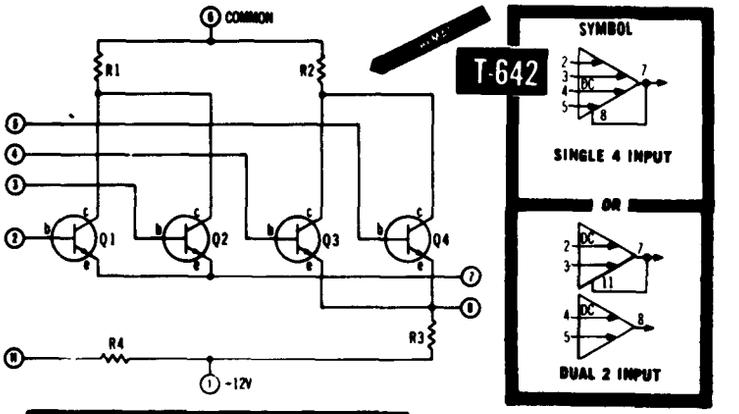


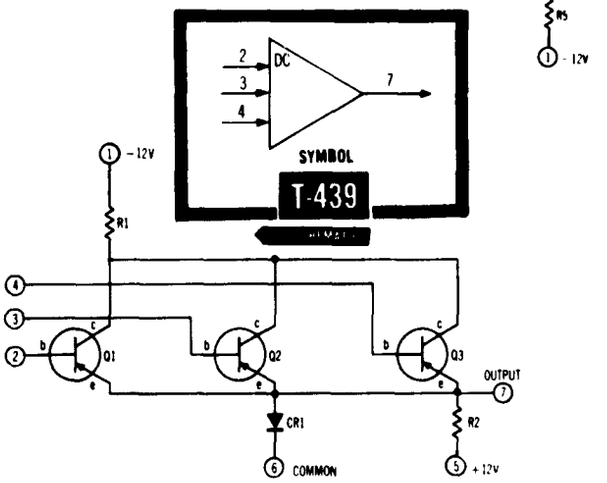


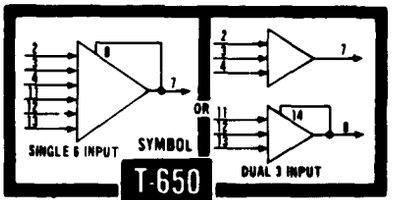


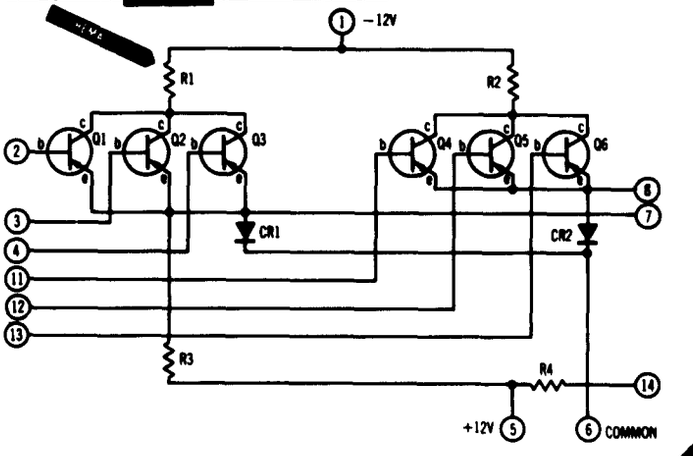


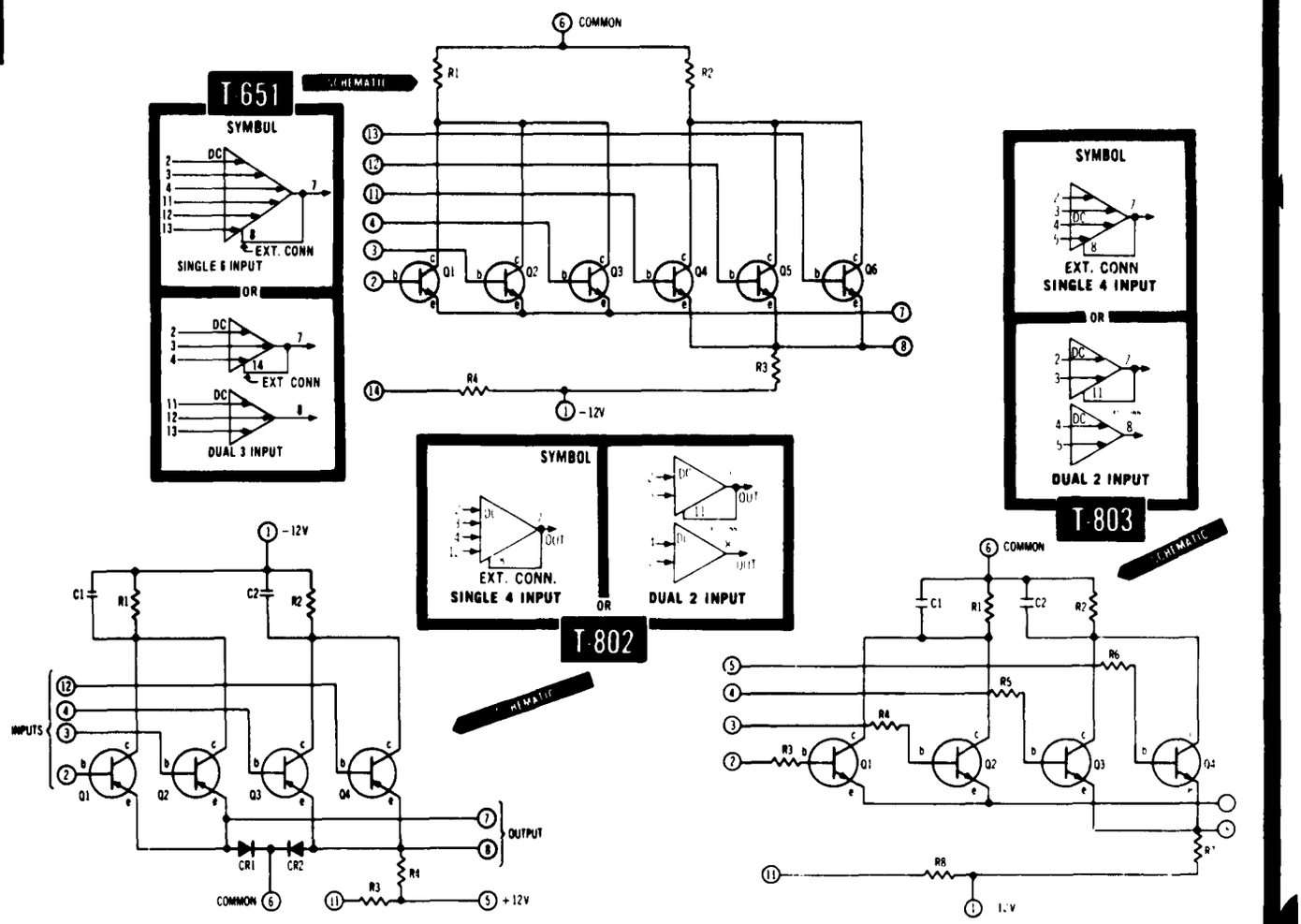












DC "And" GATES

T-404 (Dual, 2-input)
T-432 (2-input "And"/ 2-input "Exclusive-Or")
T-405 (4-input)
T-620 (Dual, 3-input)
T-621 (7-input)
T-622 (10-input)
T-627 (9-input)

DESCRIPTION

This group of logic circuits has been developed on the principle that each unit contains an integral emitter follower on the gate output. This provides superior isolation and the ability to cascade logic in almost any combination. For example, the usual diode-gate limitation that "Or" circuits cannot drive "And" circuits does not exist with these circuits.

These gates can be cascaded up to a maximum of three gates before level restoration is necessary. However, if multiple-level-"anded" terms are to be applied to a gate with terms which have not been subjected to previous "and-ing," then resistors must be used to equalize the input levels and minimize pedestal noise. Resistance values are selected according to the rule that a 560-ohm resistor between source and gate input gives a level shift approximately equal to that caused by one gate circuit. Electrical specifications for the "Exclusive-Or" section of T-432 are on the data page which describes "Exclusive-Or" gates.

ELECTRICAL SPECIFICATIONS

INPUT (each "AND" gate)

Signal Frequency Range: 0 to 250 Kc
Amplitude: −11V = "0", −3V = "1"
Input Load Characteristics:
A, B: 80, 0
C, D: 5, 25
E, F: 80, 0
Unused Inputs: In order for the gate to function, unused inputs must be connected to either −3VDC or 0V.

OUTPUT (each "AND" gate)

Amplitude: Approximately equal to input signal with level shift of +0.4 to +0.8V max.
Rise Time: For inputs with rise times faster than 0.5 μsec., output rise time is 0.5 μsec. max. For slower input rise times, output rise time equals input rise time. Rise Time Degradation, depending on input rise time and load: 0.5 to 1.0 μsec. maximum.
Drive Characteristics: These are type CD drivers. Curve IV describes drive capabilities.
Capacitive Loading: For capacitive loading, connect a 5.6KΩ external resistor from output to +12V supply.

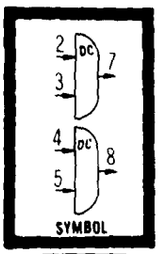
POWER REQUIRED (each "AND" gate)

−12VDC ±10%: 3.9 to 11 ma depending on load.
+12VDC ±10%: 3.9 to 11 ma depending on load.

OPERATING TEMPERATURE RANGE:
−45°C to +65°C

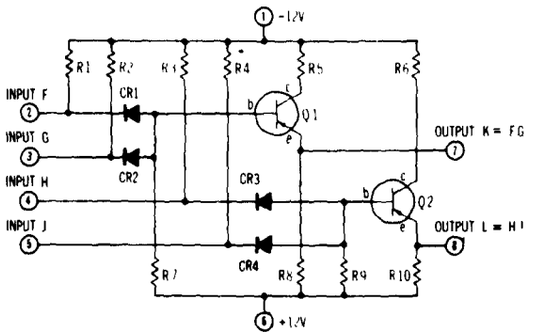
T-432

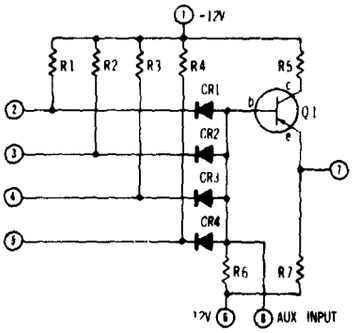
For symbol and schematic of T-432 see page 55.



T-404

SCHEMATIC

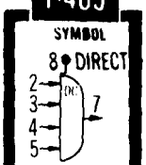


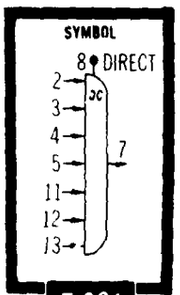


SCHEMATIC

T-405

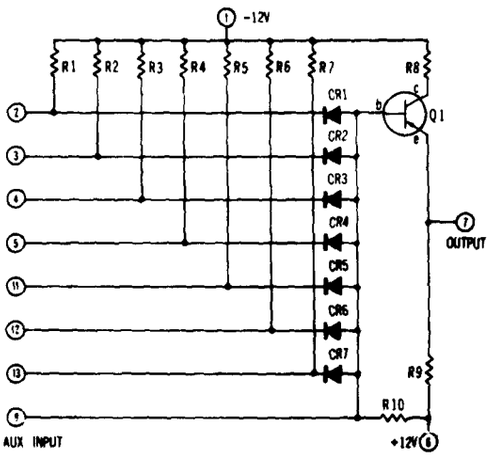
SYMBOL

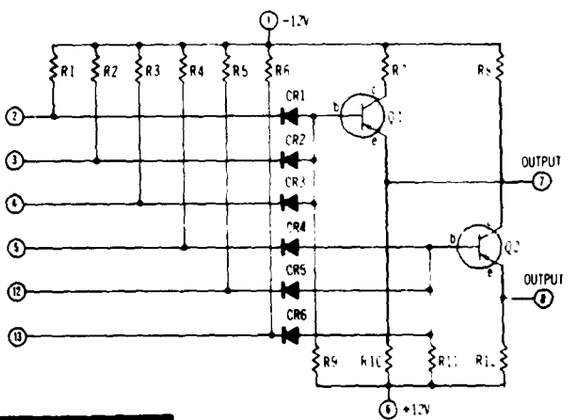




T-621

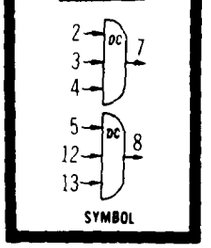
SCHEMATIC

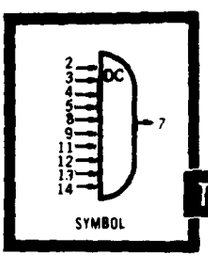




SCHEMATIC

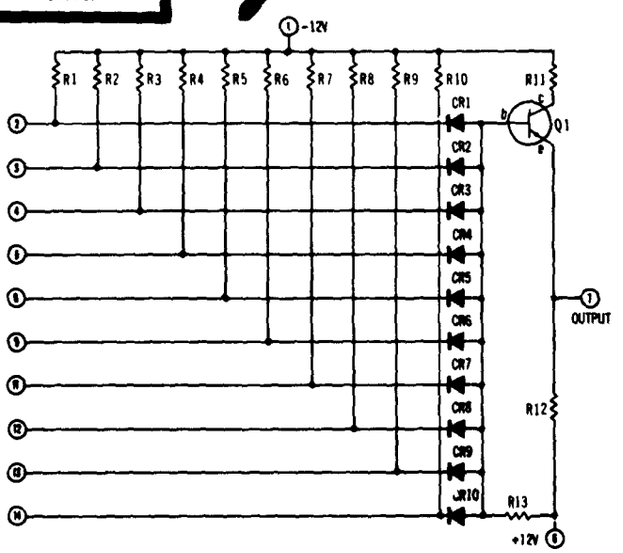
T-620





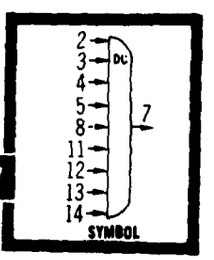
T-622

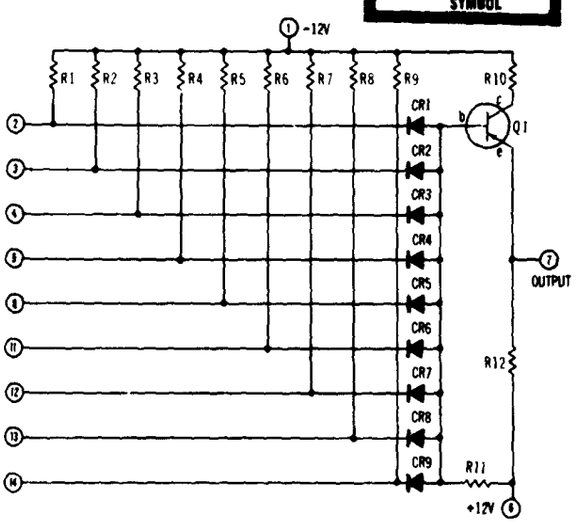
SCHEMATIC



SCHEMATIC

T-627





PULSE "And" GATES

T-318
T-410A (dual)
T-637 (dual)
T-448 (dual)
T-413 (dual with Or'ed outputs)
T-630 (triple)
T-612 (sextuple)
T-613 (sextuple, separate pulse inputs)
T-447 (2 control inputs)
T-411 (4 control inputs)
T-601 (8 control inputs)

DESCRIPTION

The purpose of a pulse gate is to permit an applied pulse to be transmitted to a load only when a control input is present. When this control input is in a binary "O" state, input pulses are grounded; when the control input is in a binary "1" state, input pulses are transmitted through the gate. These control properties have inherent delays which make the gates useful in applications where trigger and logic operations occur at the same time. The specifications give "Enable" and "Disable" delays referenced to the time at which a "turn-on" or "turn-off" signal is applied at the control input, assuming a fast-rise-time input. If the control signal has a poor waveform, these specifications on delay will not apply.

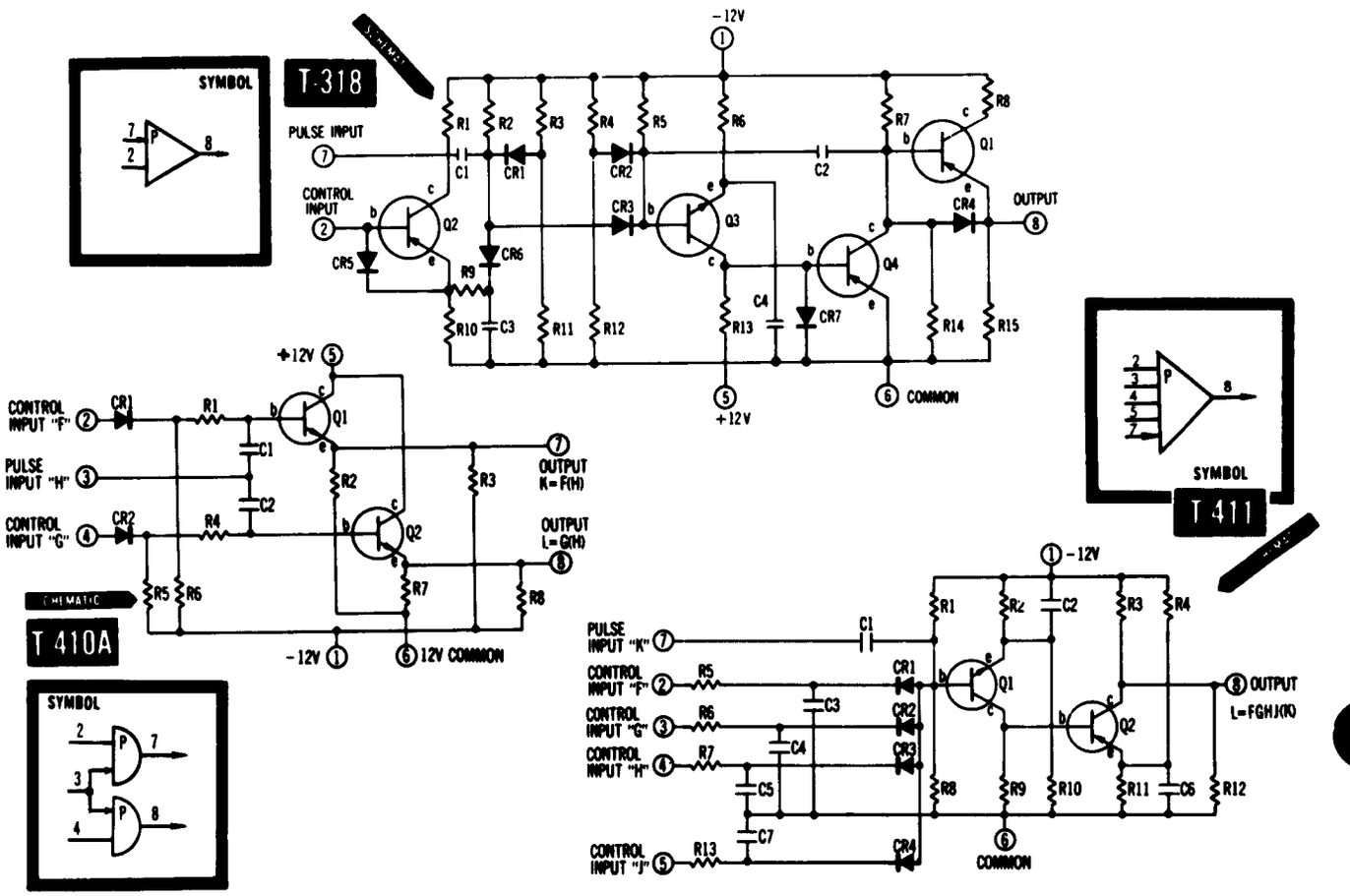
T-318 is a one-megacycle pulse "And" gate which couples gated pulses through an amplifier to produce standard 8-volt amplitude output pulses. Because of this built-in amplification, output rise time is not determined by input rise time. If additional control inputs are desired, 1-Mc DCTL "And" gates may be used to provide inputs to pin 2. T-318 may operate with pulse logic (can be cascaded with other T-318's) and can also trigger capacitive loads. Another typical application for this unit is to drive N-109 and N-110 decades.

T-410A, T-637, and **T-448** are dual pulse "And" gates; T-410A has a common pulse input, T-637 has separate pulse inputs, and T-448 has separate pulse inputs plus a built-in amplifier. Outputs of T-410A and T-637 will not normally exceed 7V peak-to-peak. However, the sharp rise time of the output and the low output impedance of the NPN emitter followers provide reliable trigger signals. These gates normally operate into capacitive loads and may be "Or" mixed but not cascaded. Features of these gates are (1) ability to be controlled directly by a flip-flop, squaring amplifier, or one-shot without need for an intervening emitter follower, and (2) output rise time is not determined by the control input.

T-413 is similar to T-637 except the gated pulses are "Or'ed" together internally. **T-630** is also similar to T-637 except it contains three gates.

T-612 and **T-613** are economical low-frequency diode pulse gates each containing six gate circuits; T-612 has a common pulse input and T-613 has separate pulse inputs. These gates are basically poor drivers but do find use in driving flip-flop base inputs directly. Additionally, if the outputs are biased to −3V these gates can be used to drive capacitive loads.

T-447, T-411, and **T-601** are multiple-control-input pulse "And" gates which transmit pulses to a load only when **all** control inputs are "true." The circuits are identical except for the number of control inputs. An integral pulse amplifier insures standardized output pulses and pulse inputs can be supplied by a pulse amplifier, squaring amplifier, blocking oscillator, or NPN emitter follower.



PULSE "And" GATES	T-318	T-410A	T-411	T-413	T-447	T-448
INPUT						
Control Input(s)						
AMPLITUDE (level shift from:)	—11 to —3V	—11 to —3V	—11 to —3V	—11 to —3V	—11 to —3V	—11 to —3V
RISE TIME	0.2 μsec max.	0.1 to 1.0 μsec	0.1 to 1.0 μsec	0.1 to 1.0 μsec	0.1 to 1.0 μsec	0.1 to 1.0 μsec
GATE ENABLE TIME (nominal)	1 μsec	2 μsec	3 μsec	2 μsec	3 μsec	3 μsec
GATE DISABLE TIME (nominal)	1 μsec	4 μsec	4 μsec	4 μsec	4 μsec	4 μsec
INPUT LOAD CHARACTERISTICS						
A, B	20, 200	10, 200	2, 200	10, 200	2, 200	2, 200
C, D	25, 100	†	†	†	†	†
E, F	20, 200	20, 200	2, 200	10, 200	2, 200	2, 200
Pulse Input(s)						
SIGNAL FREQUENCY RANGE	1 Mc max.	250 Kc max.	250 Kc max.	250 Kc max.	250 Kc max.	250 Kc max.
AMPLITUDE (P-P):	6.5V min. 9V max.	7.5V @ 0.25 μsec*	6.5V min. 9V max.	7.5V @ 0.25 μsec*	6.5V min. 9V max.	6.5V min. 9V max.
RISE TIME	.05 μsec max.	0.25 μsec max.	0.1 to 0.5 μsec	0.25 μsec max.	0.1 to 0.5 μsec	0.1 to 0.5 μsec
INPUT LOAD CHARACTERISTICS:						
A, B	10, 100	20, 200	5, 150	10, 100	5, 150	5, 150
C, D	5, 25	†	†	†	†	†
E, F	10, 100	20, 200	5, 150	10, 100	5, 150	5, 150
OUTPUT (each gate)						
AMPLITUDE (positive pulse, P-P)	8V	4.5V	8V	4.5V	8V	8V
RISE TIME	.02 μsec max.	0.25 μsec max.	0.4 μsec max.	0.25 μsec max.	0.4 μsec max.	0.4 μsec max.
PULSE DURATION (nominal)	0.3 μsec @ 250 Kc	1.1 μsec	0.5 to 3.0 μsec	1.1 μsec	0.5 to 3.0 μsec	0.5 to 3.0 μsec
LOAD DRIVE CHARACTERISTICS	C = 1000 D = 700	‡	‡	‡	‡	‡
POWER REQUIRED						
—12 VDC ±10% (peak)	30 ma	3.6 ma	6 ma	3.6 ma	9 ma	18 ma
+12 VDC ±10%	5 ma	0.8 ma	none	0.8 ma	none	none
OPERATING TEMPERATURE RANGE	—55 to +71 C	—45 to +65°C	—45 to +65 C	—45 to +65°C	—45 to +65 C	—45 to +65°C

* Lower amplitudes require faster rise times.

† Pulse "And" gates are not recommended as loads for CD drivers due to rise-time deterioration (Exception: T-318).

‡ These gates should be used only to drive capacitive loads such as flip-flops. Max. load = 5 "T" inputs, or 4 "RS" inputs.

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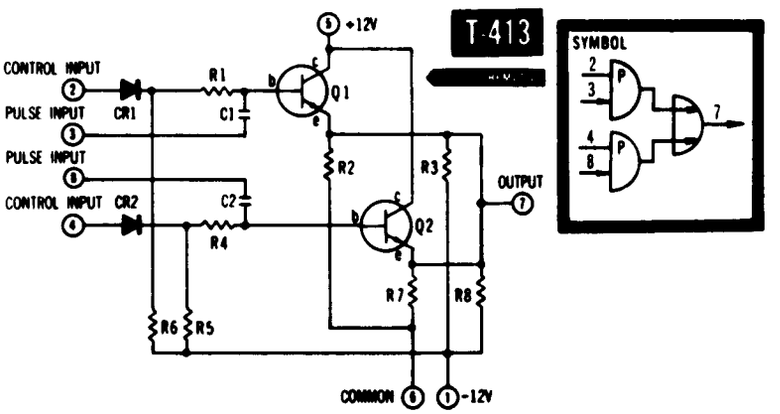

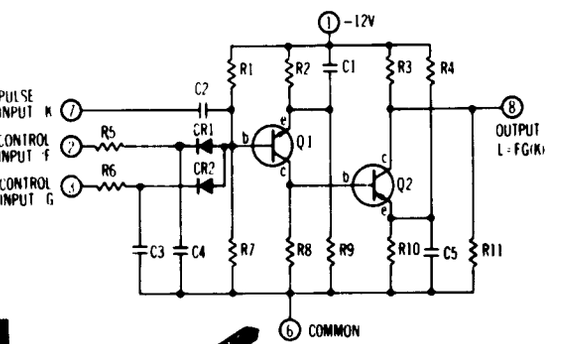

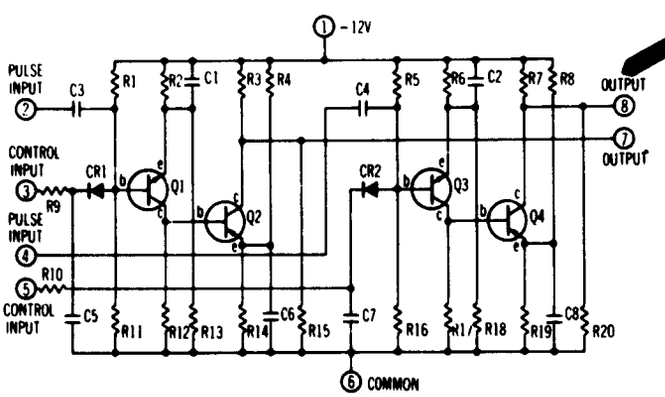

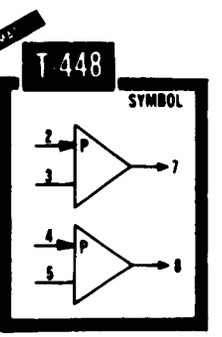

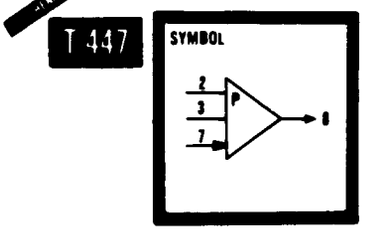

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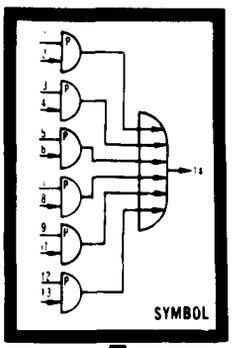
PULSE "And" GATES	T-601	T-612	T-613	T-630	T-637
INPUT					
Control Input(s)					
AMPLITUDE (level shift from:)	—11 to —3V	—11 to —3V	—11V to —3V	—11 to —3V	—11 to —3V
RISE TIME	0.2 to 1.0 μsec	0.1 to 1.0 μsec	0.1 to 1.0 μsec	0.1 to 1.0 μsec	0.1 to 1.0 μsec
GATE ENABLE TIME (nominal)	3 μsec	10 μsec	25 μsec	2 μsec	2 μsec
GATE DISABLE TIME (nominal)	4 μsec	10 μsec	25 μsec	4 μsec	4 μsec
INPUT LOAD CHARACTERISTICS					
A, B	2, 200	8, 150	8, 150	10, 200	10, 200
C, D	†	†	†	†	†
E, F	2, 200	8, 150	8, 150	10, 200	10, 200
Pulse Input(s)					
SIGNAL FREQUENCY RANGE	250 Kc max.	10 Kc max.	5 Kc max.	250 Kc max.	250 Kc max.
AMPLITUDE (P-P):	6.5V min. 9V max.	7.5V @ 0.25 μsec*	7.5V @ 0.25 μsec*	7.5V @ 0.25 μsec*	7.5V @ 0.25 μsec*
RISE TIME	0.1 to 0.5 μsec	0.25 μsec max.	0.25 μsec max.	0.25 μsec max.	0.25 μsec max.
INPUT LOAD CHARACTERISTICS:					
A, B	5, 150	80, 800	80, 800	10, 100	10, 100
C, D	†	†	†	†	†
E, F	5, 150	80, 800	80, 800	10, 100	10, 100
OUTPUT (each gate)					
AMPLITUDE (positive pulse, P-P)	8V	4.5V	4.5V	4.5V	4.5V
RISE TIME	0.4 μsec max	• input rise time	• input rise time	0.25 μsec max.	0.25 μsec max.
PULSE DURATION (nominal)	0.5 to 3.0 μsec	1.1 μsec	1.1 μsec	1.1 μsec	1.1 μsec
LOAD DRIVE CHARACTERISTICS	‡	‡	‡	‡	‡
POWER REQUIRED					
—12 VDC ±10% (peak)	6 ma	none	none	8.1 ma	3.6 ma
+12 VDC ±10%	none	none	none	1.8 ma	0.8 ma
OPERATING TEMPERATURE RANGE	—45 to +65 C	—54 to +71°C	—54 to +71 C	—45 to +65 C	—45 to +65 C

* Lower amplitudes require faster rise times.

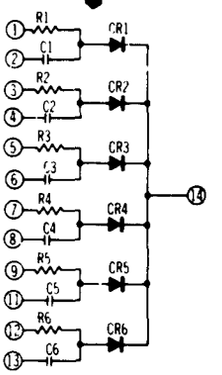
† Pulse "And" gates are not recommended as loads for CD drivers due to rise-time deterioration (Exception: T-318).

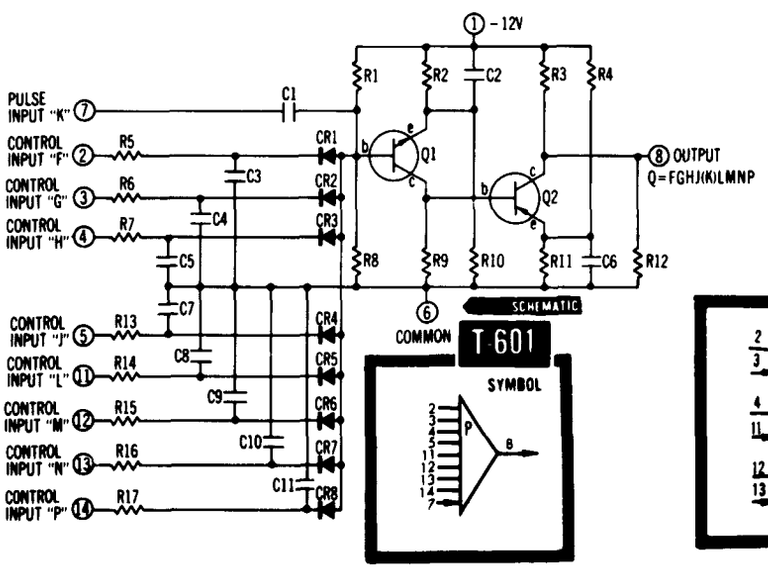
• For narrow input pulse width.

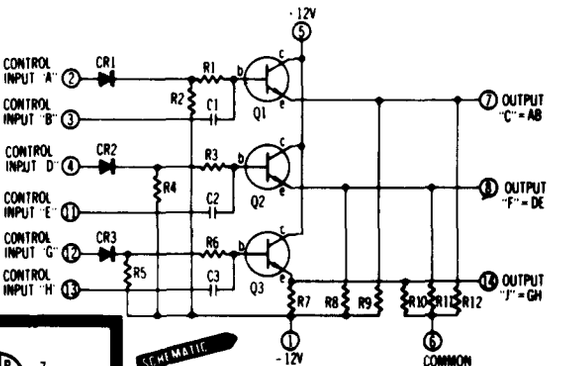
‡ These gates should be used only to drive capacitive loads such as flip-flops. Max. load = 5 "T" inputs, or 4 "RS" inputs.

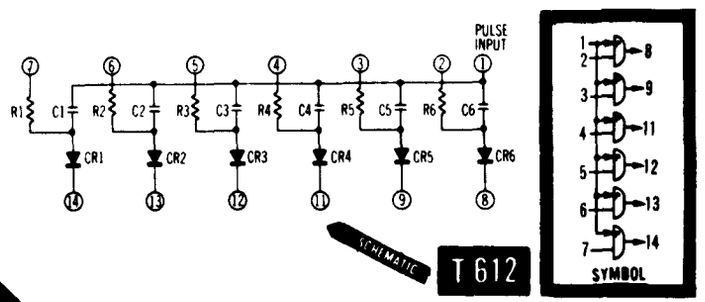


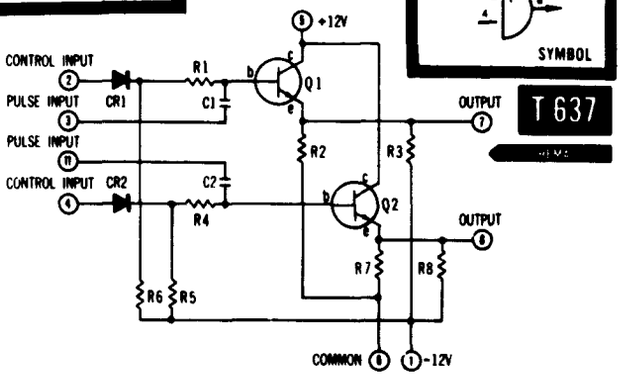
T-613











DC "Or" GATES

T-406 (Dual, 2-input)
T-407 (4-input)
T-442 (3-input)
T-614 (7-input)
T-623 (6-input)
T-634 (8-input)
T-635 (9-input)

DESCRIPTION

Design considerations for these logic circuits were similar to those for the DC "And" gates in that an integral emitter follower is used to provide circuit isolation and the ability to cascade logic in almost any combination. Two typical loads for these units are: (1) 2 parallel "Or" gates with each gate operating into 2 more parallel "Or" gates for a total logic load of 6 "Or" gates, and (2) 3 parallel "And" gates with each gate operating into 3 more parallel "And" gates for a total logic load of 12 "And" gates.

T-442 is a 3-input "Or" gate with a 2-stage level restoring circuit and an emitter-follower output; basically a cascaded combination of one-half of a T-406, a T-106, and a T-111. This unit was designed to provide level restoration in the "Carry" line of parallel adders and subtracters. Normally, this level restoration is necessary after every third operation.

ELECTRICAL SPECIFICATIONS

INPUT (Each "Or" gate)

Signal Frequency Range: 0 to 250 Kc
Amplitude: −11V = "0", −3V = "1"
Input Load Characteristics (all units except T-442)
A, B: 90, 0
C, D: 5, 25
E, F: 90, 0
Input Load Characteristics of T-442
A, B: 250, 200
C, D: 25, 400
E, F: 250, 200
Unused Inputs: Connect unused inputs to pin 1 (−12VDC)

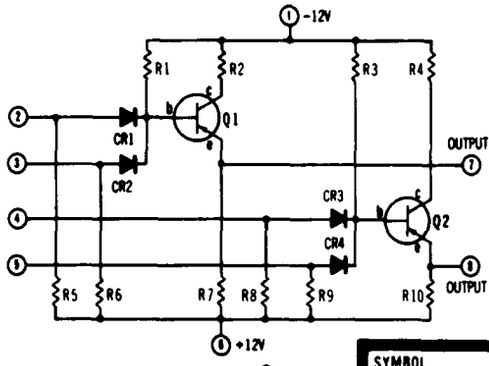
OUTPUT (Each "Or" gate)

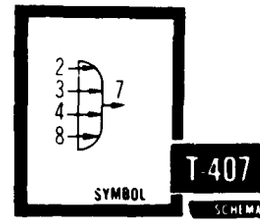
Amplitude: Approximately equal to input signal. T-442 causes negligible level shift; all other units produce a level shift of +0.1V.
Rise Time: For inputs with rise times faster than 0.5 μsec, output rise time is 0.5 μsec. max. For slower input rise time, output rise time equals input rise time. Rise Time Degradation, depending on input rise time and load: 0.5 to 1.0 μsec. maximum.
Drive Characteristics: These are type CD drivers. Curve IV describes drive capabilities.
Capacitive Loading: For capacitive loading, connect a 5.6KΩ external resistor from output to +12V supply.

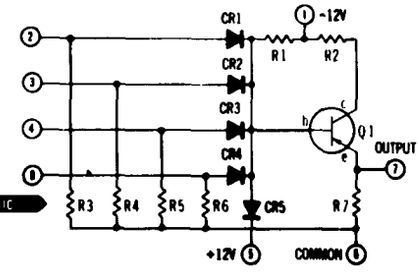
POWER REQUIRED (Each "Or" gate)

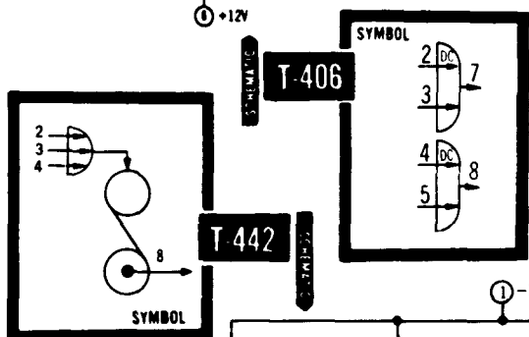
−12VDC ±10%: 3.9 to 11 ma depending on load. T-442 requires 12 to 20 ma.
+12VDC ±10%: 3.9 to 11 ma depending on load. T-442 requires a maximum of 12 ma.

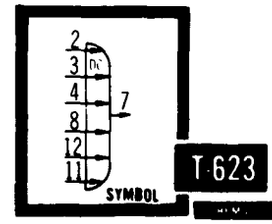
OPERATING TEMPERATURE RANGE:
−45 C to +65 C

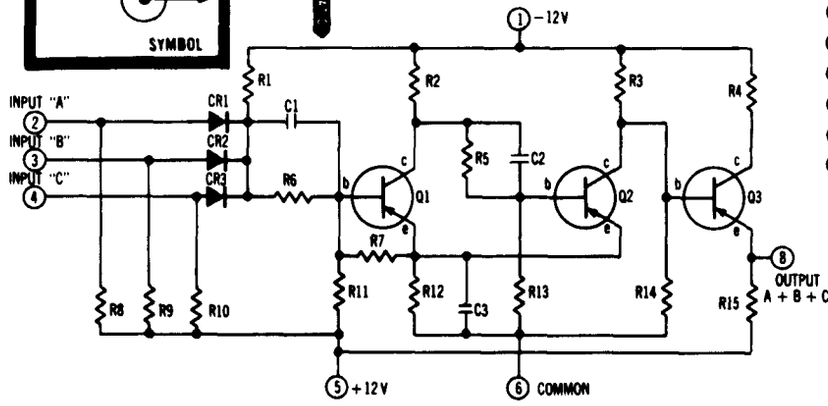


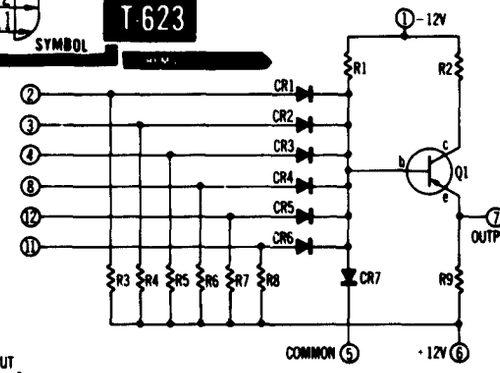












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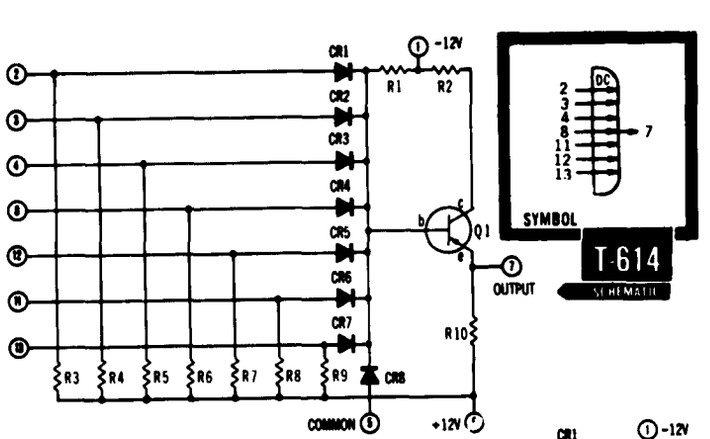
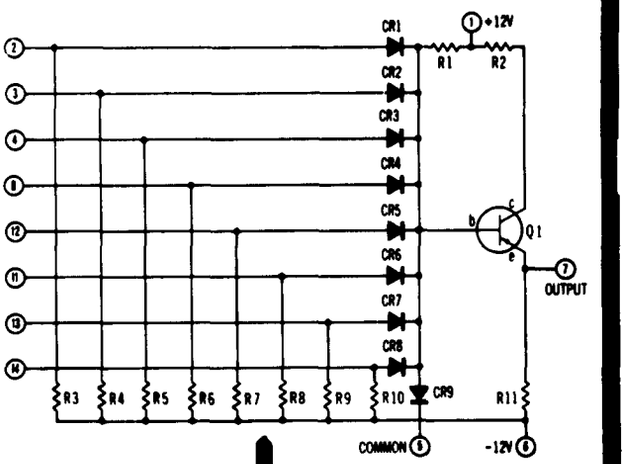
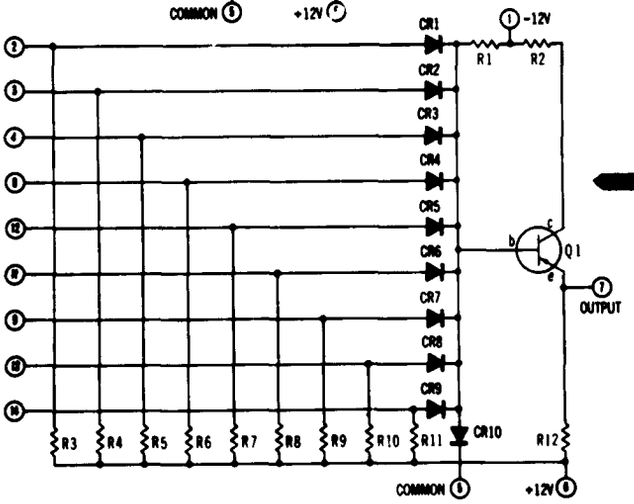
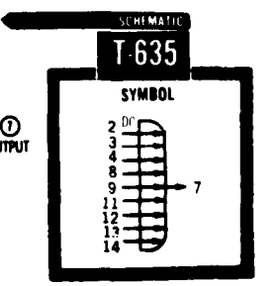








EXCLUSIVE-"Or" GATES
T-315, T-421A, T-422, T-423A, T-432, T-805

DESCRIPTION

The purpose of an "exclusive-Or" gate is to provide an output when one and only one input is "true." Logic equations for all gates except T-422 are: $X = A\bar{B} + \bar{A}B$

and, for dual gates, the second equation is:

$$Y = E\bar{F} + \bar{E}F$$

Since T-422 is a 3-input gate, the equation for T-422 is:

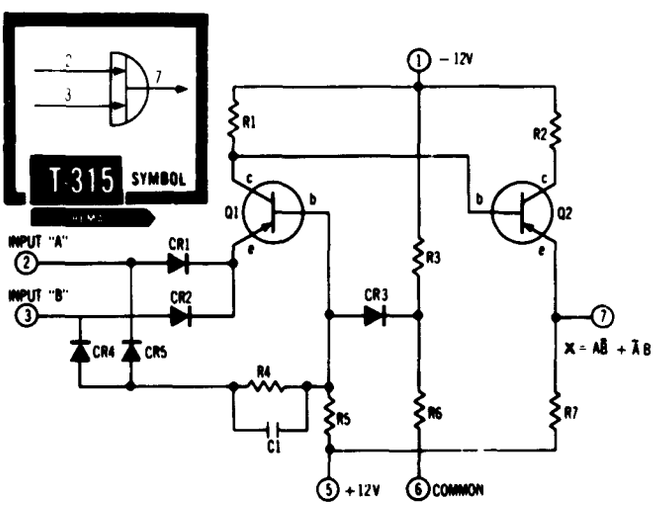
$$X = A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C$$

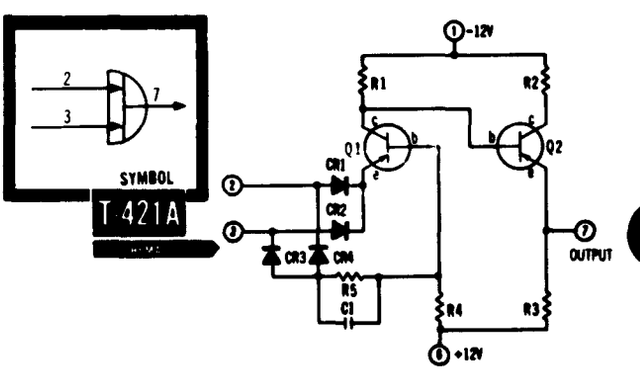
The time delay between input and output signal excursions, measured between half-amplitude points, is 1.5 μsec maximum for one 250-Kc gate or 2.0 μsec maximum for two cascaded 250-Kc gates. Corresponding delays for the 1-Mc gates are 0.5 μsec maximum for one gate or 0.7 μsec maximum for two cascaded 1-Mc gates. In order to determine the maximum possible accumulated delay (T in μsec) through N cascaded "exclusive-Or" gates, use one of the following equations:

250Kc GATES	1Mc GATES
T = N (if N is even)	T = 0.35N (if N is even)
T = N + 0.5 (if N is odd)	T = 0.35N + 0.15 (if N is odd)

These circuits can be used as logic inverters by holding one input at −3 volts (ON) while a second input is switched ON and OFF by the signal that is to be inverted. Output rise time is now a function of the input fall time and the β of Q_1.

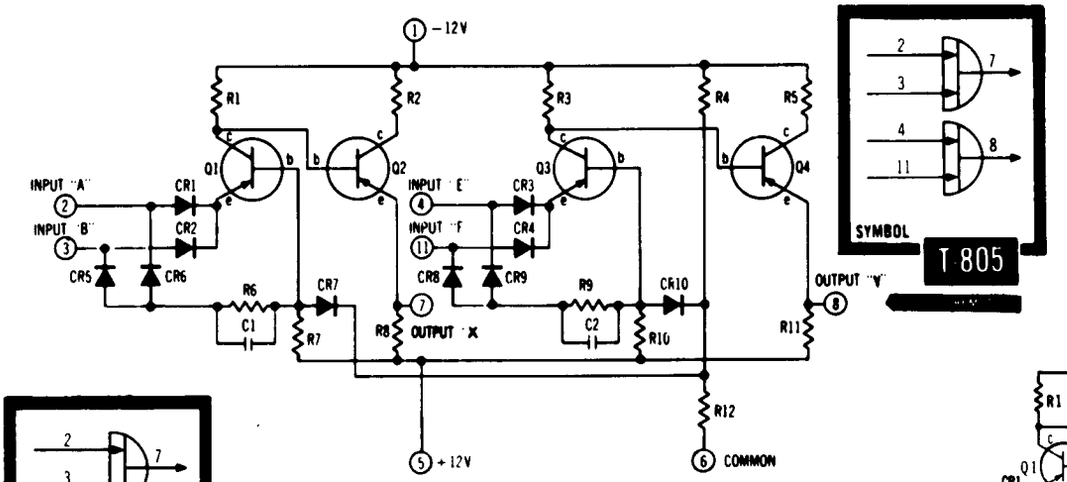
A PNP-emitter-follower output circuit is recommended for driving these "exclusive-Or" gates. If the desired driving circuit does not have a PNP-emitter-follower configuration at its output, connect the driving circuit output to a T-111 (or equivalent) and the output of the T-111 to the input of the "exclusive-Or" gate.





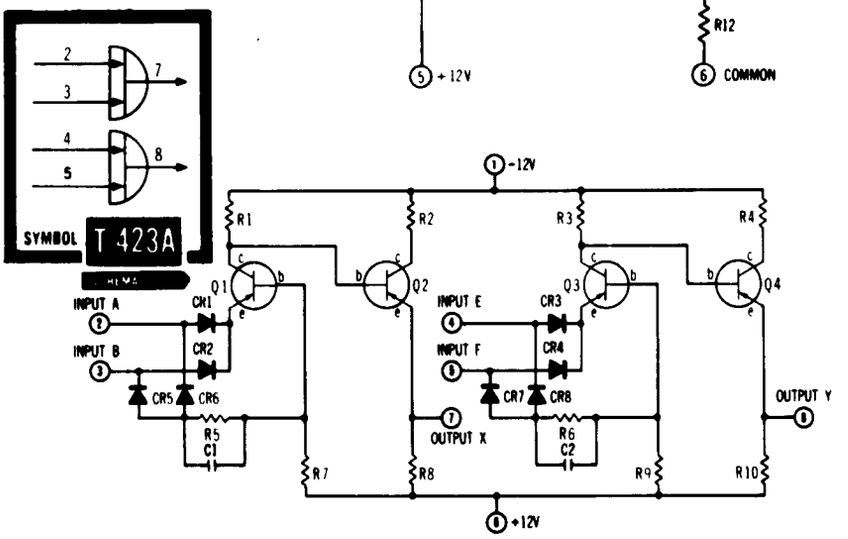
EXCLUSIVE—"Or" GATES	T-315 2-Input	T-421A 2-Input	T-422 3-Input	T-423A Dual, 2-Input	T-432* 2-Input "And"/ 2-Input Exclusive-"Or"	T-805 Dual, 2-Input
INPUT						
SIGNAL FREQUENCY RANGE	0 to 1 Mc	0 to 250 Kc	0 to 250 Kc	0 to 250 Kc	0 to 250 Kc	0 to 1 Mc
AMPLITUDE (a level shift from:)	—11V (±1) to —3V (±0.6)	—11V (±1) to —3V (±1)	—11V (±1) to —3V (±0.6)	—11V (±1) to —3V (±0.6)	—11V (±1) to —3V (±0.6)	—11V (±1) to —3V (±0.6)
INPUT LOAD CHARACTERISTICS:						
A, B	15, 200	35, 0	35, 0	35, 0	15, 200	15, 200
C, D	5, 25	5, 25	5, 25	5, 25	5, 25	5, 25
E, F	15, 200	35, 0	35, 0	35, 0	15, 200	15,200
Rise and Fall Time (max.)	2.0 μsec	2.5 μsec	2.0 μsec	2.5 μsec	2.5 μsec	2.0 μsec
OUTPUT						
AMPLITUDE	—11V = "0", —3V = "1"	—11V = "0", —3V = "1"	—11V = "0", —3V = "1"	—11V = "0", —3V = "1"	—11V = "0", —3V = "1"	—11V = "0", —3V = "1"
LEVEL SHIFT:						
Typical	—0.15V	—0.15V	—0.2V	—0.15V	—0.15V	—0.15V
Maximum	—0.25V	—0.25V	—0.3V	—0.25V	—0.25V	—0.25V
RISE TIME	0.5 μsec max.	1.0 μsec max.	1.0 μsec max.	1.0 μsec max.	1.0 μsec max.	0.5 μsec max.
DELAY TIME, INPUT TO OUTPUT (See "Description")	0.5 μsec max.	1.5 μsec max.	2 μsec typ	1.5 μsec max.	1.5 μsec max.	0.5 μsec max.
DRIVE CHARACTERISTICS (Max.)	C = 200, D = 400	C = 200, D = 400	C = 200, D = 400	C = 200, D = 400	C = 200, D = 400	C = 200, D = 400
POWER REQUIRED						
—12VDC ± 10%	8 ma	6 ma	9 ma	12 ma	(Including "And" section:) 3.9 to 11 ma depending on load	16 ma
+12VDC ± 10%	6 ma	6 ma	8 ma	12 ma	3.9 to 11 ma depending on load	12 ma
OPERATING TEMPERATURE RANGE	—54 to +71 C	—54 to +71°C	—54 to +71 C	—54 to +71°C	—45 to +65°C	—54 to +71°C

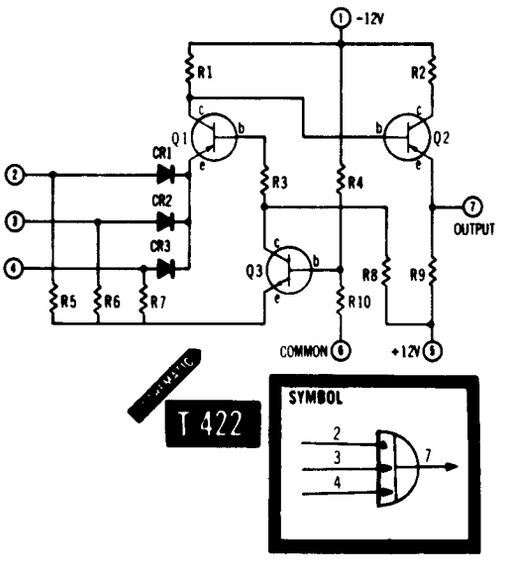
*These specifications are for the "exclusive—Or" section of T-432. For the "And" section of T-432, see DC "And"



T 432

For symbol and schematic of T-432 see page 55.





PULSE "Or" GATES/MIXER AMPLIFIERS

T-430 (2-input) **T-412 (5-input)**
T-431 (3-input) **T-602 (9-input)**

DESCRIPTION

These are multiple-input pulse mixers or "Or" gates with an integral pulse amplifier to produce standardized output pulses. Inputs may be either voltage steps or pulses; a fast-rise-time output pulse is produced each time an input pulse or step is applied to any of the inputs.

External R-C networks and blocking diodes may be connected to the pin-5 input of T-431 to give additional mixing capability.

ELECTRICAL SPECIFICATIONS

INPUT

Amplitude: Minimum input is a 7.0-volt positive pulse or step at rise times as long as 0.8 μsec. Circuits will respond to lower-amplitude inputs at faster rise times but will **not** respond to 1.5V or less regardless of rise time.

Signal Frequency Range: 250Kc maximum.

Input Impedance: 270pf maximum.

Input Characteristics:

A	B	C	D	E	F
10	100	0	200	10	100

OUTPUT

Amplitude: 8.5V peak-to-peak positive pulse from −11VDC to −2.5VDC.

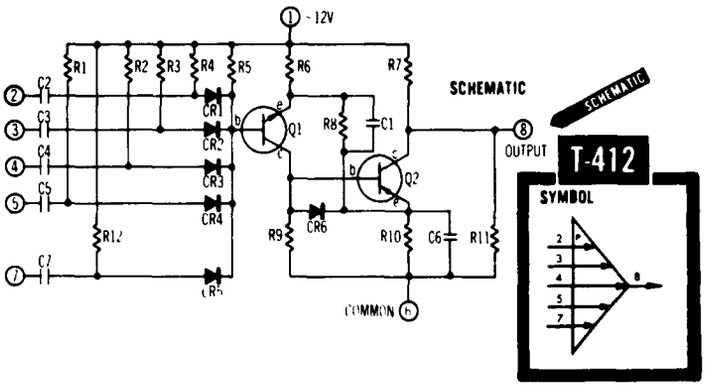
Rise Time: 0.4 μsec maximum into a capacitive load.

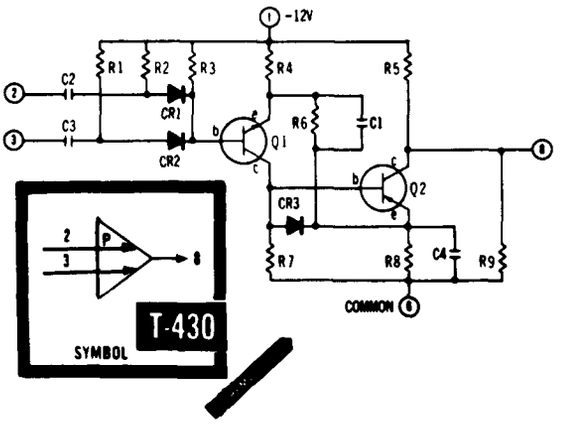
Duration: 0.5 to 2.0 μsec

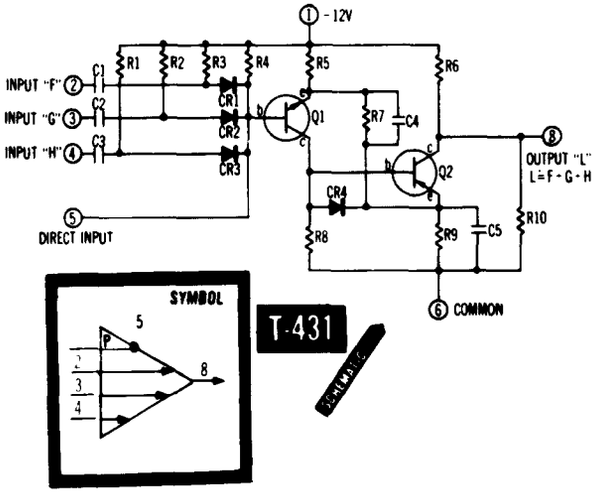
Drive Characteristics: These are type AB drivers. Curve XIII describes drive capabilities.

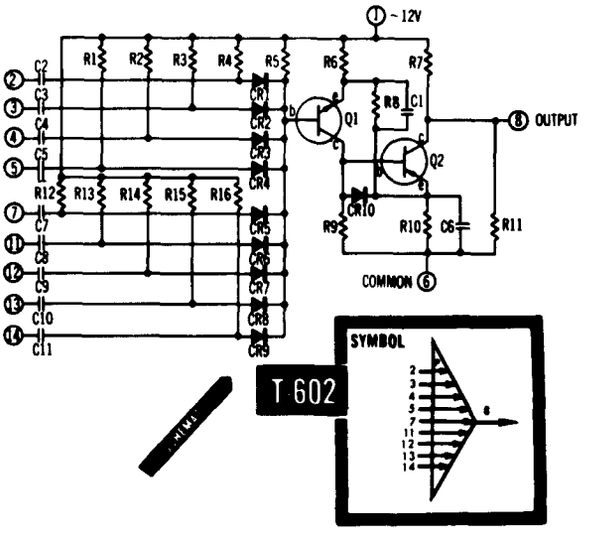
POWER REQUIRED: −12VDC, ±10%: 2 ma quiescent, 10 ma peak

OPERATING TEMPERATURE RANGE:
−45°C to +65°C









"And"/"Or" GATES
T-432, T-433, T-434, T-653

DESCRIPTION

T-432 is a dual logic unit consisting of a 2-input DC "And" gate and a 2-input "Exclusive-OR" gate. Specifications for the "Exclusive-OR" section are contained on the "Exclusive-OR" data sheet elsewhere in this catalog.

T-433 is a dual logic unit that contains a 2-input DC "And" gate and a 2-input DC "Or" gate. This unit is basically one-half of a T-404 and one-half of a T-406

T-434 is a dual 2-input DC "And" gate with "Or'ed" output. If the inputs are defined as A (pin 2), B (pin 3), C (pin 4), and D (pin 5), then the output is logically defined as AB + CD.

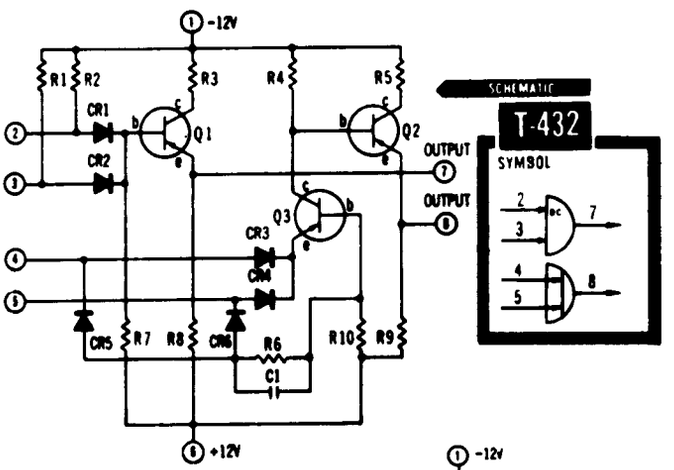
T-653 is a dual logic unit which consists of a 2-input DCTL "And" gate and a 2-input DCTL "Or" gate. The circuits are similar to those discussed on the data sheet describing other DCTL logic units. Essentially, this unit is one-half of a T-641 and one-half of a T-642.

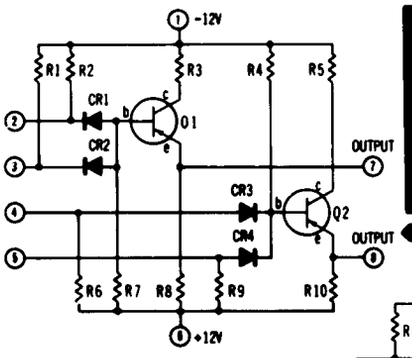
"AND"/"OR" GATES	T-432 2-Input "And"/2-input "Exclusive-Or"*	T-433 2-input "And"/2 input "Or"	T-434 Dual 2-input "And" with "Or'ed" output	T-653 DCTL logic 2-input "And"/ 2-input "Or"
INPUT				
SIGNAL FREQUENCY RANGE	0 to 250 Kc	0 to 250 Kc	0 to 250 Kc	0 to 250 Kc
AMPLITUDE	—11V = "0", —3V = "1"	—11V = "0", —3V = "1"	—11V = "0", —3V = "1"	—11V = "0", —3V = "1"
INPUT LOAD CHARACTERISTICS:				
A, B	80, 0	80, 0	90, 0	And: 10, 0 Or: 10, 25
C, D	5, 25	5, 25	5, 25	And: 8, 0 Or. 5, 25
E, F	80, 0	80, 0	90, 0	And: 10, 0 Or: 10, 25
OUTPUT				
AMPLITUDE (approx)	★	★	★	equal to input
LEVEL SHIFT	+0.4V	And: +0.4V Or: +0.1V	+0.3V	And: +0.3V Or: —0.25V
RISE TIME (depending on input rise time)	0.5 to 1.0 μsec	0.5 to 1.0 μsec	0.5 to 1.0 μsec	0.2 μsec max
DRIVE CHARACTERISTICS†	CD type IV	CD type IV	CD type IV	And: CD type IV Or: EF type VIII
POWER REQUIRED				
—12 VDC ± 10% (depending on load)	each gate 17 ma	each gate 3.9 to 11 ma	4.5 to 13 ma	4.9 to 18 ma
+12 VDC ±10% (depending on load)	17 ma	3.9 to 11 ma	4.5 to 13 ma	3.9 to 11 ma
OPERATING TEMPERATURE RANGE	—45 to +65 C	—45 to +65°C	—45 to +65°C	—54 to +71°C

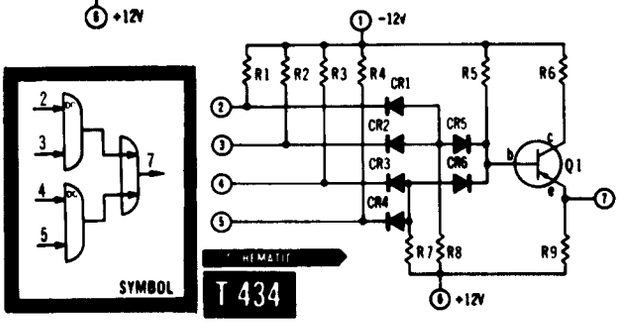
*Specifications for "Exclusive-Or" section are on table titled "Exclusive-Or" Gates

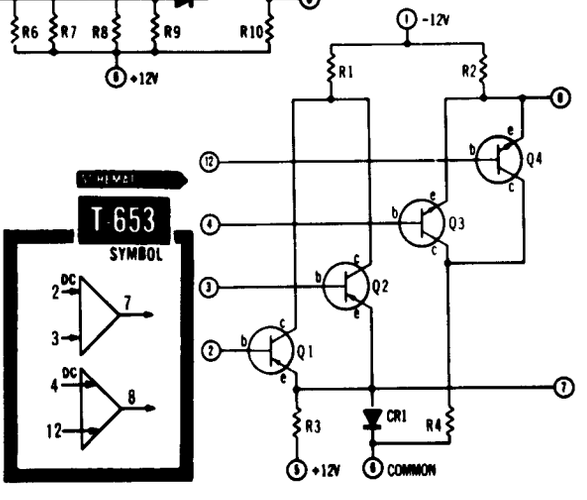
†When "And" gates are to drive capacitive loads, connect an external 5.6 KΩ resistor from output to 12V supply.

★ For inputs with rise time faster than 0.5 μsec., output rise time is 0.5 μsec. max. For slower input rise times, output rise time equals input rise time.









"Nor" and "Nand" GATES
T-308, T-437, T-438, T-645

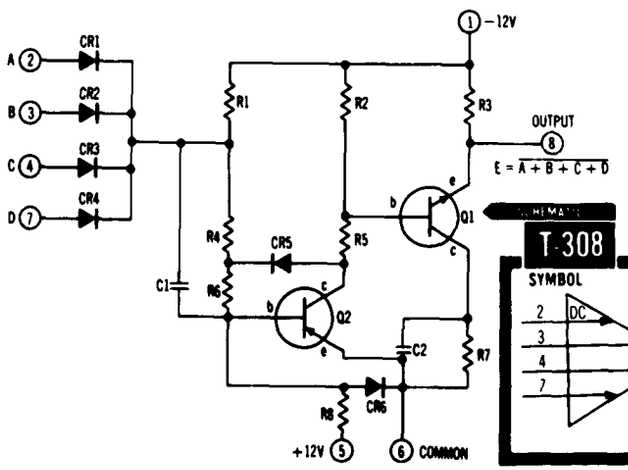
DESCRIPTION

"Nor" and "Nand" Gates are versatile logic circuits which provide "not-Or" ("Nor") and "not-And" ("Nand") functions. For example, NOR Gate T-437 consists of a 4-input "Or" gate operating into an inverting amplifier. The inverter provides both inversion and level restoration. Outputs are from an integral PNP emitter follower and thus no interstage coupling element is necessary between gates or between gates and amplifiers.

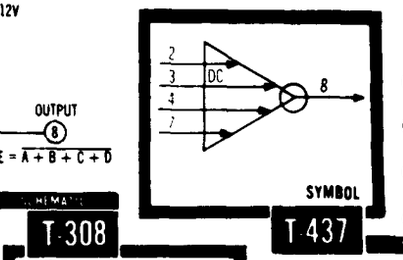
DTL circuits used overcome a major short-coming of conventional R-C input circuits in the "Nor" gates. That is, when one input signal is at the "1" level and the remaining inputs are all switching simultaneously, the output will remain in the "0" state.

"NOR"/"NAND" GATES	T-308 (4-input "Nor")	T-437 (4-input "Nor")	T-438 (4-input "Nand")	T-645 (7-input "Nor")
INPUT				
SIGNAL FREQUENCY RANGE	0 to 1 Mc	0 to 250 Kc	0 to 250 Kc	0 to 250 Kc
AMPLITUDE (±1V)	—3V = "1" —11 V = "0"	—3V = "1" —11 V = "0"	—3V = "1" —11 V = "0"	—3V = "1" —11 V = "0"
RISE TIME	.05 to 0.2 μsec	0.1 to 1.0 μsec	0.1 to 1.0 μsec	0.1 to 1.0 μsec
INPUT LOAD CHARACTERISTICS				
A, B	30, 50	20, 100	70, 300	30, 50
C, D	100, 100	100, 100	5, 25	100, 100
E, F	15, 20	5, 20	70, 300	5, 20
OUTPUT				
AMPLITUDE (unloaded, ±1V)	—3V to —11V	—3V to —11V	—3V to —11V	—3V to —11V
MAXIMUM RISE TIME (under typical load, less loading will yield faster rise time)	0.2 μsec	1.0 μsec	1.0 μsec	1.0 μsec
DRIVE CHARACTERISTICS	EF type XV*	EF type XVII*	CD type IV†	EF type XVII*
POWER REQUIRED				
+12 VDC (±10%)	1.0 ma	0.5 ma	5.5 ma	0.5 ma
—12 VDC (±10%)	7.5 ma	6.0 ma	9 ma	6.0 ma
OPERATING TEMPERATURE RANGE	—55 to +71°C	—54 to +71°C	—54 to +71°C	—54 to +71°C

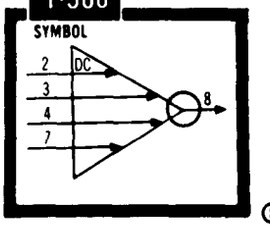
*When driving capacitive loads, connect a 5.6 KΩ external resistor from output to —12V supply.
†When driving capacitive loads, connect a 5.6 KΩ external resistor from output to +12V supply.

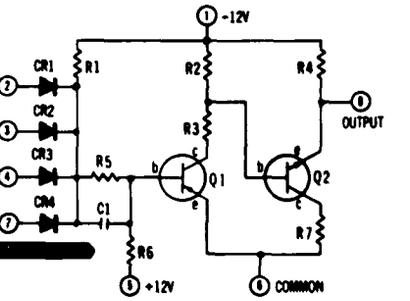


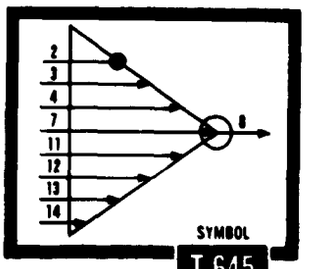
T-308



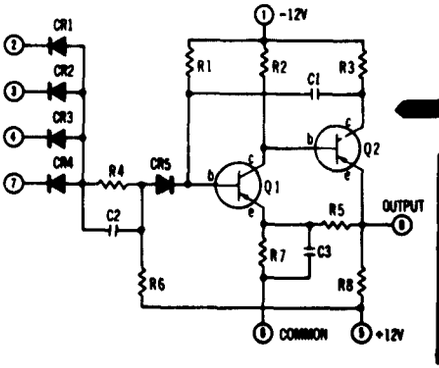
T-437



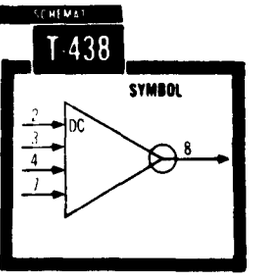


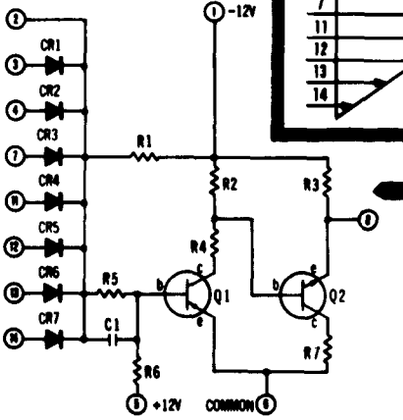


T-645



T-438





T 645

MULTIVIBRATORS T-104, T-166, T-167, T-314

DESCRIPTION

T-104 and **T-314** are general-purpose multivibrators used to generate square waves and time-base frequencies. The operating frequency is established by use of external timing capacitors. Equations which describe the approximate relationship between period of oscillation T (in μsec) and the value of two external capacitors C_x (in pf) are as follows:

T-104	T-314
$C_x = 45(T\text{-}2.6)$	$C_x = 75(T\text{-}1)$

T-104 can operate in either a free-running or a synchronized mode; T-314 has no provision for external synchronization. Additionally, to provide frequency multiplication, T-104 can be synchronized by an input frequency somewhat lower than the frequency of oscillation. Frequency multiplication by factors of 2, 3, 4, or 5 are possible at output rates as high as 150 Kc. This is accomplished by using the input pulse rate to synchronize the multivibrator at a frequency slightly higher than the free-running frequency of the multivibrator. If, for example, it is desired to multiply an input 5Kpps pulse rate to a 25Kpps output pulse rate, charging capacitors C_x would be selected such that the circuit would free-run at approximately 24.7Kc. Input 5Kpps pulses then force the circuit to operate at 25Kc. The chart below defines the nominal harmonic relationship of the synchronizing (locking) signal to the MV output. Figures shown in the right-hand column are the percentage deviations (from the free-running frequency) over which reliable locking can be obtained.

SYNC/FREE-RUN FREQ.	LOCKING RANGE
F	0 to +20%
2f	0 to +12%
f 2	0 to +7%
f 3	0 to +4.5%
f 4	0 to +3.5%
f 5	0 to +2.5%

When locked at 2F, output loading is restricted to pin 8 only.

MULTIVIBRATORS	T-104	T-166 (One-Shot)	T-167 (One-Shot)	T-314
INPUT				
SIGNAL FREQUENCY RANGE	0 to 325 Kc	0 to 250 Kc	0 to 250 Kc	— No Input — Natural frequency is 1 Mc (+0.3 Mc to —0.1 Mc)
AMPLITUDE:				
Will respond to positive pulse inputs of:	6.0V or more	6.0V or more	6.0V or more	—NA—
at rise times up to:	1.0 μsec max.	1.0 μsec max.	1.0 μsec max.	—NA—
Will not respond to inputs of: regardless of rise time.	1.5V or more	1.5V or more	1.5V or more	—NA—
Maximum amplitude	9V	9V	9V	—NA—
RISE TIME:	0.1 to 1.0 μsec*	0.1 to 1.0 μsec*	0.1 to 1.0 μsec*	—NA—
INPUT LOAD CHARACTERISTICS:				
A, B	10, 100	10, 100	10, 100	—NA—
C, D	8, 75	8, 75	8, 75	—NA—
E, F	10, 100	10, 100	10, 100	—NA—
OUTPUT				
AMPLITUDE (nominal level shift from:)	—11V to —3V	—11V to —3V	—11V to —3V	—11V to —3V
RISE TIME (nominal, under typical load)	0.4 μsec	0.5 μsec	0.2 μsec	0.3 μsec under max. load at 100 Kc
FALL TIME	Approx. 25% of period	pin 7: Nominal 20% of pulse duration Pin 8: Nominal 1.5 μsec	Pin 7: Nominal 1.5 μsec Pin 8: Nominal 20% pulse duration	0.2 μsec max.
PULSE DURATION	See Description	See Description	See Description	See Description
Minimum Period	2.6 μsec typical	Approx. 2.0 μsec	1.5 μsec	1 μsec††
Maximum Period	60 sec†	1 sec ‡	1 sec	10 μsec††
DUTY CYCLE				
To 50 Kc	—NA—	70% max.	70% max.	—NA—
To 250 Kc	—NA—	50% max.	50% max.	—NA—
LOAD DRIVE CHARACTERISTICS	AB type XII	AB type XI	AB type XI	AB type XIX
POWER REQUIRED				
—12 VDC ±10%	5.5 ma	7 ma	5.5 ma	22 ma
OPERATING TEMPERATURE RANGE	—45 to +65°C	—45 to +65°C	—45 to +65°C	—54 to +71°C

* For inputs with rise times slower than 1.0 μsec, use an external capacitor of appropriate size and connect to direct input.

† Equation in DESCRIPTION valid only for periods up to 1 second.

‡ For duty cycles greater than 50%, pulse duration is shorter.

†† The period may be decreased by use of external resistors connected across pins 3 and 1 and pins 5 and 1. Minimum values for these resistors are 10 KΩ. The value of these resistors should be determined experimentally for the desired period between 1 and 10 μsec. Dynamic values of resistance may be used to frequency-modulate T-314.

continued on next page

T-166 and **T-167** are one-shot multivibrators. Primary functions of these units include pulse-width generation, time delay, and temporary digit storage. T-166 contains a built-in noise rejection circuit which minimizes the inherent noise sensitivity of one-shot circuits. T-167 has been specifically designed to provide a minimum of pulse width variation over the temperature range. **T-167 is superior to T-166** for pulse-width-stability over the temperature range but **T-166 is superior to T-167** for pulse-width-stability under power supply voltage changes.

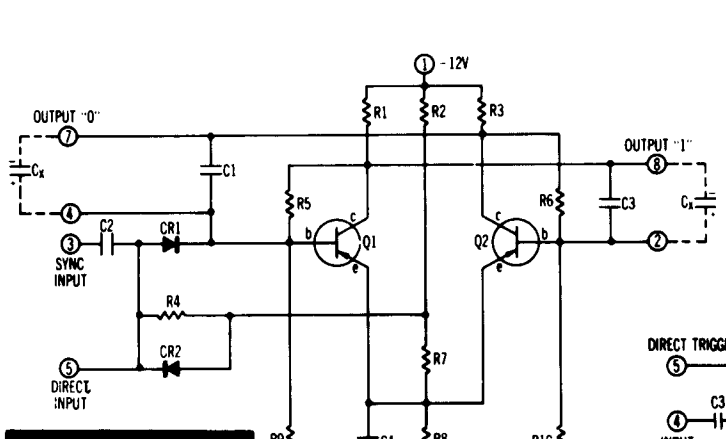
Both circuits are triggered by a positive pulse or positive-going input step. Outputs are two rectangular pulses of opposite polarity. The time duration of output pulses is determined by an externally connected capacitor. Pulse widths from 2 μsec to 1 second are obtainable at duty cycles up to 70%. The approximate relations between pulse duration and capacity are given by the following equations:

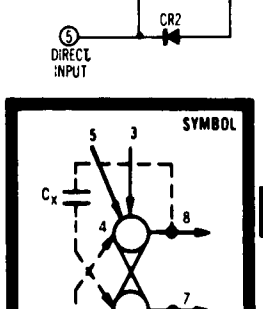
T-166	**T-167**
$C_x = \frac{60(T-2)}{}$	$C_x = \frac{100(T-2)}{}$

T in μsec
C_x in pf

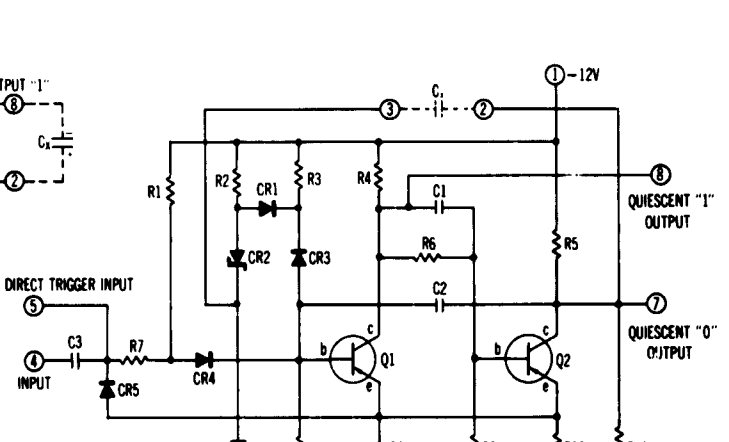
For duty cycles greater than 50%, pulse width is slightly narrower than the equation indicates.

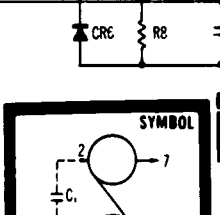
When a polarized capacitor is used, the positive terminal should connect to Pin 3.



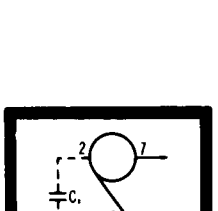


T-104

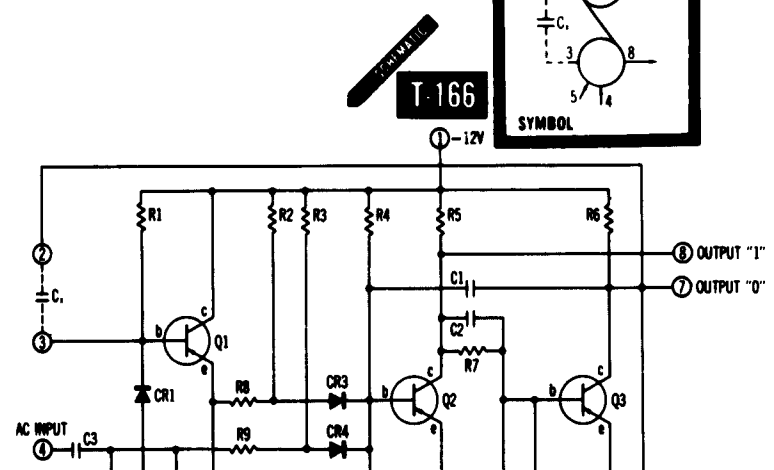


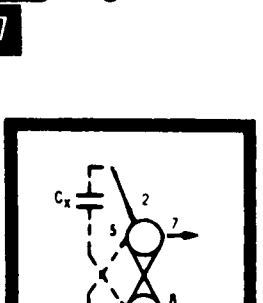


T-167

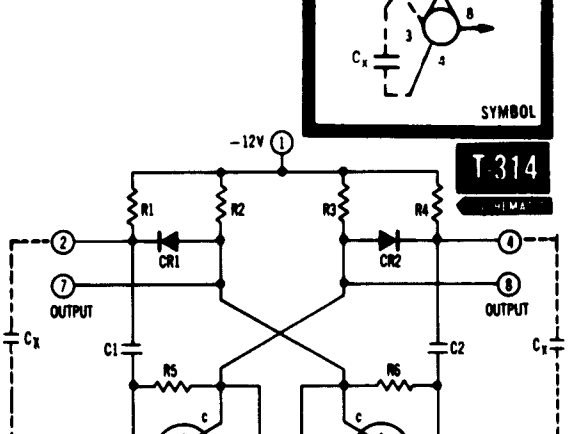


T-166





T-314



CRYSTAL CONTROLLED OSCILLATORS
T 107, T 127, T 140, T 311

DESCRIPTION

These units are transistorized crystal-controlled oscillators which have square-wave outputs at the crystal resonant frequency. These units are normally supplied without crystals but, as a service, EECo can supply certain specific crystals from stock; these crystals are described in the paragraphs which describe specific circuits with which they can be used. Special crystals for other frequencies can be supplied, but, a 3-month delivery is normal and these crystals must be quoted by the factory. When requesting a quotation, please state operating frequency, "spot" tolerance, frequency stability, and ambient temperature range.

To achieve maximum stability, an oven should be used to contain both the circuit and the crystal. These ovens are also described in the paragraphs which describe the specific circuits with which they can be used.

T-107 consists of a two-stage saturated feedback amplifier with an NPN emitter follower output. The unit, when used with an appropriate crystal, is capable of operating anywhere within the frequency range of 10Kc to 75Kc. (For operation in the range of 10Kc to 45Kc, jumper pin 4 to pin 5.) The crystal is used in a series resonant mode to achieve maximum stability and acts as the coupling impedance between the output of the second amplifier stage and the input of the first stage. Since a full 360° phase shift occurs through two cascaded common-emitter transistor amplifiers, the circuit oscillates without appreciable phase shift or attenuation through the crystal.

H-145-31 is a 10Kc crystal which can be used with T-107. Specifications for this crystal are as follows:

Drive Level: 0.1 milliwatt

Maximum Motional Resistance: 100KΩ

Frequency: 10Kc

Calibration Accuracy: +0.000%, −0.004%

Reference Temperature: +70°C

Max. Temp. Coeff. at Ref. Temp.: −4 parts per million per °C

Holder Type: MC-13A

Type of Cut: +5°X

To achieve a maximum frequency stability of ±0.0005%, both the T-107 and the associated crystal should be installed in an oven. Two ovens can be used with T-107; **H-149** when operating in the frequency range of 10Kc to 45Kc, and **H-150** when operating in the frequency range of 45Kc to 75Kc. These ovens are contained in rectangular packages which plug into octal tube sockets and basic specifications are presented below.

SPECIFICATION	H-149	H-150
Operating Temperature	+70°C(±1°)	+70°C(±1°)
Temp. Stability:		
slowly-varying ambient	±1°C	±1°C
constant ambient	±0.2°C	±0.2°C
Ambient Range	−54 to +65°C	−54 to +65°C
Warm-up Time at −54°C ambient	15 min.	15 min.
Power Consumed	40 watts	40 watts
External Dimensions (approx. length x width x seated height)	2-1/4" x 2" x 3-5/16"	2-1/4" x 2" x 3-5/16"
Cavity Dimensions (approx. length x width x height)	1-3/4" x 1-3/8" x 2-1/4"	1-3/4" x 1-3/8" x 2-1/4"

These ovens are available with a choice of two heater voltages; H-149-1 and H-150-1 have 115V AC/DC heaters and H-149-2 and H-150-2 have 28V AC/DC heaters.

Frequency Trimming to achieve small changes in operating frequency are permissible by addition of an external capacitor C_A or C_B as shown in Figure 1. Table 1 present some typical frequency changes for values of C_A and C_B.

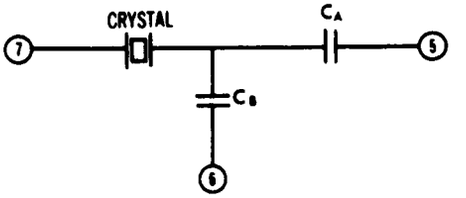


FIG. 1. Frequency Trimming Method

Table 1. Frequency Change vs. Trimming Capacitance (T-107)

ΔF (%)	C_A (pf)	C_B (pf)
+0.0010	170	NO CONNECT.
+0.0005	400	NO CONNECT.
+0.0002	700	NO CONNECT.
−0.0002	Jumper	160
−0.0005	Jumper	300
−0.0010	Jumper	500

T-127 consists of a Butler oscillator circuit with an NPN emitter follower output. The unit, when used with an appropriate crystal, is capable of operating anywhere within the frequency range of 75Kc to 250Kc. The crystal is used in a series resonance mode to achieve maximum stability and acts as the coupling impedance between the two stages of the Butler circuit. Since one stage is a common-collector circuit and the other is a common-base circuit, (a 0° phase shift through the cascaded CC-CB stages) oscillation occurs without appreciable phase shift or attenuation through the crystal.

H-146-2 is a 100Kc crystal which can be used with T-127. Specifications for this crystal are as follows:

Drive Level: 2 milliwatts

Maximum Motional Resistance: 2.5KΩ

Frequency: 100Kc

Calibration Accuracy: +0.000%, −0.002%

Reference Temperature: +70°C

Max. Temp. Coeff. at Ref. Temp.: −2.5 parts per million per °C

Holder Type: MC-13A

Type of Cut: +5°X

continued on next page

T-127 *(continued)*

To achieve a maximum frequency stability of ±0.0003% under maximum combined variations of temperature, supply voltage, and load, both the T-127 and the associated crystal should be installed in an H-150 oven. Characteristics of this oven have already been described. Frequency Trimming with an external capacitor can be accomplished as shown in Figure 1. Table 2 presents some typical frequency changes for values of C_A and C_B.

Table 2. Frequency Change vs. Trimming Capacitance (T-127)

F (%)	C_A (μf)	C_B (μf)
+0.0010	0.003	NO CONNECT.
+0.0005	0.007	NO CONNECT.
−0.0005	Jumper	0.003
−0.0010	Jumper	0.005

T-140 consists of a two-stage saturated feedback amplifier and a two-stage squaring amplifier. The unit, when used with an apropriate crystal, is capable of operating anywhere within the frequency range of 1Kc to 10Kc (For operation in the range of 1Kc to 2Kc, jumper pin 3 to pin 5; for 2Kc to 5Kc, jumper pin 4 to pin 5; and for 5Kc to 10Kc, no jumper is required.) The crystal is operated in a series resonant mode to achieve maximum stability and the circuit operates similarly to T-107. Crystals to operate at frequencies as low as 1Kc are very difficult to procure because of the relatively large size of the crystal. However, **H-167-8** is a 1Kc crystal which can be used with T-140. Specifications for this crystal are as follows:

Drive Level: 0.1 milliwatt
Maximum Motional Resistance: 200KΩ
Frequency: 1.0Kc
Calibration Accuracy: ±0.005%
Reference Temperature: + 20°C
Max. Temp. Coeff. at Ref. Temp.: ±1 part per million per °C
Holder Type: T-500
Type of Cut: +5°X

Frequency trimming with an external capacitor can be accomplished as shown in Figure 1. Table 3 presents some typical frequency changes for values of C_A or C_B.

Table 3. Frequency Change vs. Trimming Capacitance (T-140)

Δ F (%)	C_A (μf)	C_B (μf)
+0.0010	0.003	NO CONNECT.
+0.0005	0.005	NO CONNECT.
+0.0002	0.01	NO CONNECT.
−0.0002	Jumper	0.01
−0.0005	Jumper	0.02
−0.0010	Jumper	0.05

T-311 consists of a Butler oscillator circuit, a PNP saturated amplifier, and a PNP emitter follower output circuit. This unit, when used with an appropriate crystal, is capable of operating anywhere within the frequency range of 250Kc to 1Mc. (For frequencies below 900Kc, jumper pin 4 to pin 5. For frequency of 900 Kc and above, jumper pin 1 to pin 2.) The crystal operates in a series resonant mode to achieve maximum stability and the circuit operates similarly to T-127.

H-160-10 is a 1Mc crystal which can be used with T-311. Specifications for this crystal are as follows:

Drive Level: 2 milliwatts
Maximum Motional Resistance: 1KΩ
Frequency: 1 Mc
Calibration Accuracy: ±0.001%
Reference Temperature: +70°C
Max. Temp. Coeff. at Ref. Temp.: ± 1 part per million per °C
Holder Type: MC-6A
Type of Cut: AT

To achieve a maximum frequency stability of ±0.0003% (3 parts in 10⁴), both the T-311 and the associated crystal should be installed in an oven. Two ovens can be used with T-311; **H-149** when operating in the frequency range of 250Kc to 899.99Kc, and **H-150** when operating in the frequency range of 900Kc to 1Mc. Characteristics of these ovens were described in the description of T-107.

Frequency trimming with an external capacitor can be accomplished as shown in Figure 1. Table 4 presents some typical frequency changes for values of C_A or C_B.

Table 4. Frequency Change vs. Trimming Capacitance (T-311)

Δ F (%)	C_A (μf)	C_B (μf)
+0.0010	0.0006	NO CONNECT.
+0.0005	0.0015	NO CONNECT.
−0.0005	Jumper	0.0003
−0.0010	Jumper	0.0006

CRYSTAL CONTROLLED OSCILLATORS	T-107	T-127	T-140	T-311
OUTPUT				
FREQUENCY RANGE	10 Kc to 75 Kc*	75 Kc to 250 Kc	1 Kc to 10 Kc†	250 Kc to 1 Mc‡
FREQUENCY STABILITY: ††				
Circuit only	±0.005%	±0.001%	±0.001%	±0.002% •
With Unit and Crystal in Oven	±0.0005%	±0.0003%	±0.0005%	±0.0003% •
AMPLITUDE: 8V level shift from	—11 to —3V	—11 to —3V	—11V to —3V	—11 to —3V
RISE TIME: (μsec)	0.1 to 1.0	0.4 to 1.0	0.05 to 1.0	0.05 max.
LOAD DRIVE CHARACTERISTICS	EF type XVII	EF type XVII	AB type I	AB type XXI
POWER REQUIRED				
—12 VDC ±10%	7 ma	10 ma	20 ma	12 ma
OPERATING TEMPERATURE RANGE	—54 to +71 C	—54 to +71°C	—54 to +71 C	—54 to +71°C

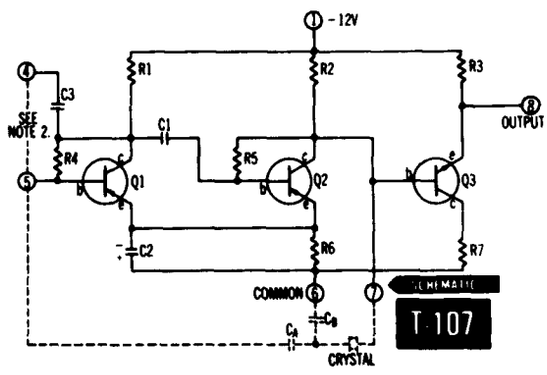
* For operation in range 10 Kc to 45 Kc, jumper pin 4 to 5.

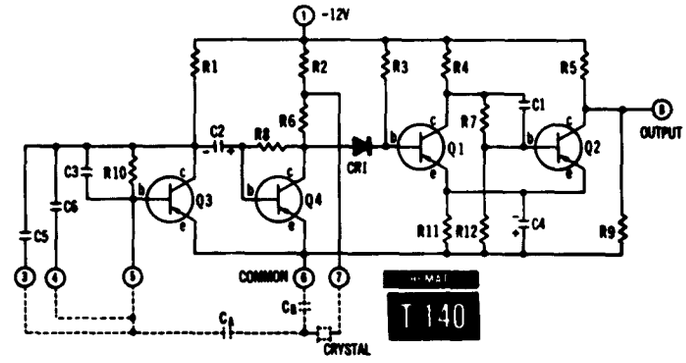
† For operation in range 1 Kc to 2 Kc, jumper pin 3 to pin 5; and for operation in range 2 Kc to 5 Kc, jumper pin 4 to pin 5.

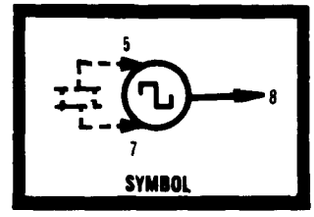
‡ For operation at frequencies below 900 Kc, jumper pin 4 to pin 5 and for operation in range 900 Kc to 1 Mc, jumper pin 1 to pin 2.

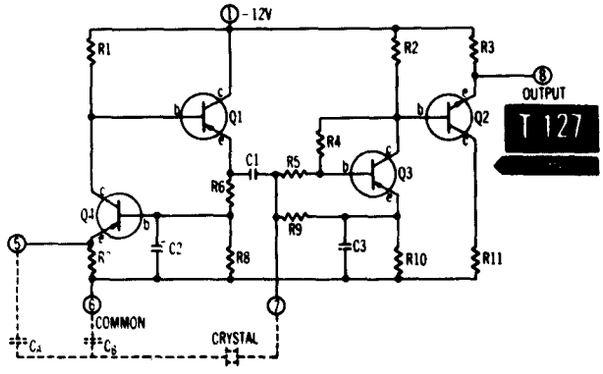
†† Short term stability due to maximum combined variations of temperature, supply voltage, and load.

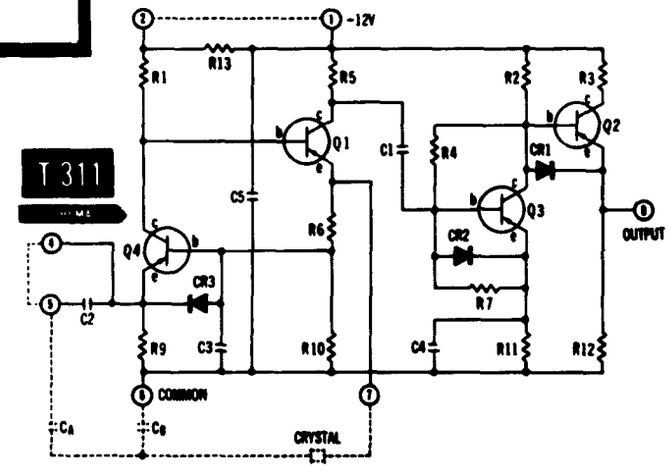
• ±0.001% if temp. limits are —20°C to +71°C.











BLOCKING OSCILLATOR T 110

DESCRIPTION

T-110 is a blocking oscillator using two transistors in a monostable circuit. When triggered, the T-110 generates a sharp positive pulse capable of driving a heavy capacitive load.

ELECTRICAL SPECIFICATIONS

INPUT:

Signal Frequency Range: 0 to 250Kc

Trigger Amplitude:

Minimum: Will always operate on positive-going pulse of 6V or more at rise times as long as one microsecond. Faster rise times will allow lower-amplitude trigger signals but the circuit will **not** trigger on any positive-going pulse of 1.5V or less regardless of rise time.

Maximum: 9V P-P

Rise Time: 0 1 to 1.0 μsec

Input Load Characteristics:

A, B: 25, 100
C, D: 30, 130
E, F: 25, 100

OUTPUT:

Amplitude (unloaded): 8V P-P from −11VDC to −3VDC

Polarity: Positive

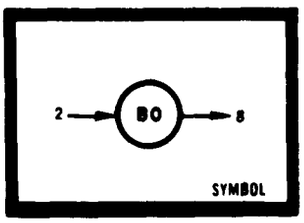
Rise Time: 0.1 μsec to 0.8 μsec depending on load

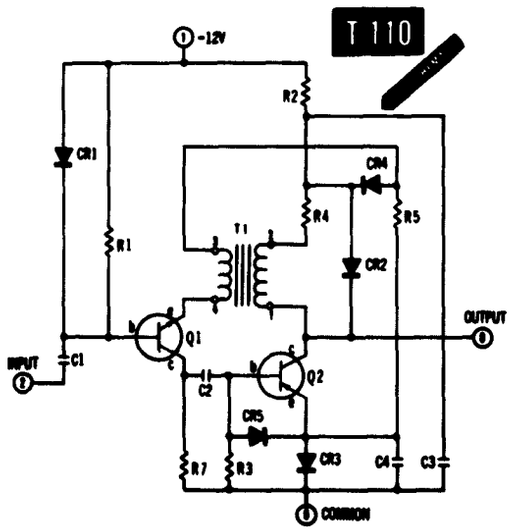
Duration: 0.5 to 2.0 μsec depending on input amplitude. (Pulse duration is narrower with lower input amplitudes.)

Load Drive Characteristics: This is an AB type driver capable of driving 1000 A units and 5000 B units.

POWER REQUIRED: −12VDC ±10% at 12 ma quiescent and at 40 ma peak.

OPERATING TEMPERATURE RANGE: −45 to +65°C





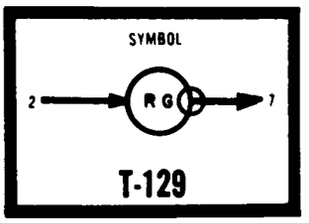
RESET GENERATORS T 109, T 129

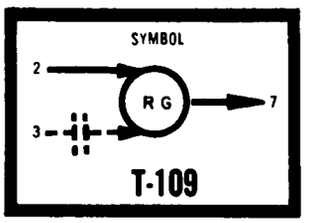
DESCRIPTION

Reset Generator T-109 is designed to reset (or set) T-Series type flip-flops and Reset Generator T-129 is designed to reset N-Series type decades.

In use, the **T-109** output is applied to the direct reset (or set) input of the flip-flops concerned. When an ON signal (nominally −3VDC) is applied to the T-109, one of the transistors in each flip-flop is held in a cut-off condition suspending normal flip-flop operation. When an OFF signal (nominally −11VDC) is applied to the T-109, the flip-flops will respond normally to input signals. The **T-129** similarly suspends operation of decades but, in this case, does so by saturating one transistor in each N-Series flip-flop (Refer to "Use of Reset Generators" in the "Family Information" section of this catalog.)

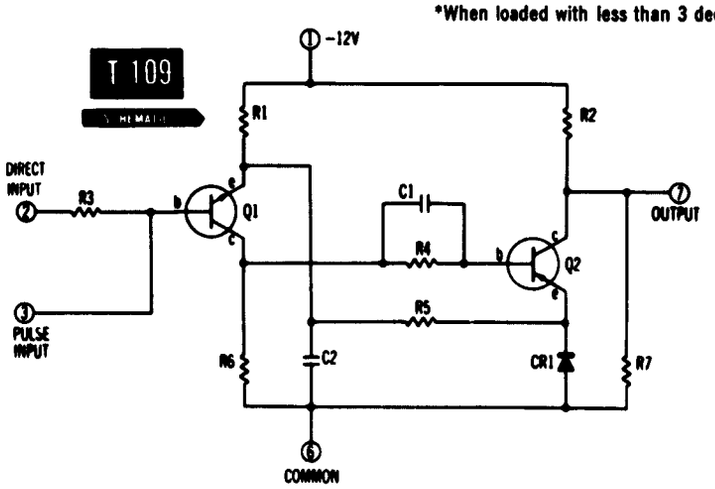
The standard input for these units is an 8-volt DC level shift (−11 to −3VDC) such as would be obtained from a flip-flop, one-shot, or gate. Push-button switches can also be used if care is taken to avoid "contact bounce" problems. Pulse resetting may also be employed.

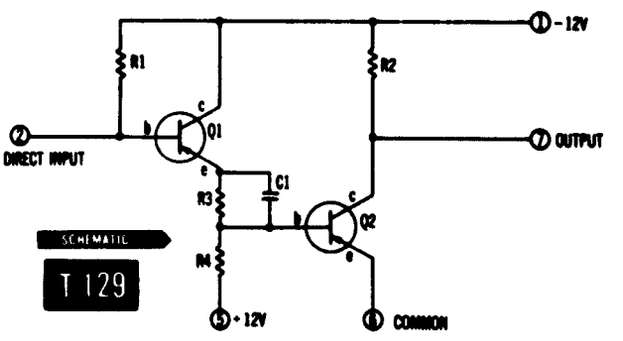




RESET GENERATORS	T-109 (for T-series)	T-129 (for N-series)
INPUT		
SIGNAL FREQUENCY RANGE	0 to 250 Kc	50 Kc max with N-Series
AMPLITUDE:		
Direct Input (Level Shift)	min: —9 to —4 VDC max: —12 to 0 VDC	min: —9.5 to —4 VDC max: —12 to 0 VDC
Pulse Input		
Minimum Pulse or Level Shift	7V P-P through external capacitor to pin 3	7V P-P through external capacitor (470 pf capacitor→ 15 μsec output pulse)
Rise Time	0.1 to 0.6 μsec	1.0 μsec max
Add connections necessary:	(1) 33 KΩ external resistor between pins 3 and 6 (2) External jumper between pins 1 and 2	(1) None
INPUT LOAD CHARACTERISTICS:		
A, B	pin 2: 5, 50 pin 3: 30, 50	10, 25
C, D	pin 2: 5, 25 pin 3: 5, 25	5, 25
E, F	pin 2: 5, 50 pin 3: 10, 25	10, 25
OUTPUT		
AMPLITUDE (Level shift from:)		
Unloaded	—5 to —0.3 VDC	0 to —12 VDC
Max. Load	—4 to —0.3 VDC	0 to —4 VDC
DURATION	1 μsec min. to DC	15 μsec min. to DC
RISE TIME (Nominal)	0.5 μsec	0.5 μsec
FALL TIME (Nominal)	0.5 μsec	DC Input: 1 μsec AC Input: ¼ input pulse width
LOAD DRIVE CHARACTERISTICS	AB Driver Max A =100 Max B =200	*AB Driver Max A =1000 Max B =2000
POWER REQUIRED		
—12VDC ±10%	quiescent: 3 ma during reset: 7 ma	quiescent: 20 ma during reset: 13 ma
+12VDC ±10%	None	1.5 ma
OPERATING TEMPERATURE RANGE	—45 to +65°C	—54 to +71°C

*When loaded with less than 3 decades, insert 1 KΩ resistor in series with output.





VOLTAGE REGULATOR T-123

DESCRIPTION

T-123 is a shunt-type, regulated, negative 7.5-volt supply. A medium-power zener diode is used yielding low output impedance and good regulation. Three ranges of regulated current are available by means of an external jumper.

The usual application for T-123 is to supply bias for neon type Minisig® indicators when they are used with T-Series units. This bias shifts the Minisig operating characteristics to accommodate the output signal levels of T-Series circuits. Table 1 lists permissible neon Minisig loads for the three current ranges established by an external jumper.

Table 1

Load Units	No Jumper	Jumper Pins 1 & 2	Jumper Pins 1, 2, & 3
R-101 R-121	6	13	20
R-201 R-221	3	6	10

ELECTRICAL SPECIFICATIONS

OUTPUT:

Voltage Level: −7.5VDC (±1.0V)

Regulated Output Current:

No Jumper: 0 to 6 ma

Jumper between Pins 1 & 2: 12 ma

Jumper between Pins 1 & 2 & 3: 18 ma

Impedance: Approximately 10Ω

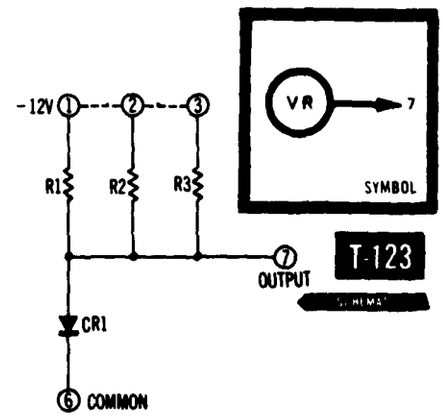
POWER REQUIRED: −12VDC ±10%

No Jumper: 22 ma

Jumper between Pins 1 & 2: 44 ma

Jumper between Pins 1 & 2 & 3: 66 ma

OPERATING TEMPERATURE RANGE: −45 to +65°C



BIAS SUPPLY T-173

DESCRIPTION

This unit provides −3VDC and −11VDC bias voltages. The circuit has been designed to draw current to a positive source; if it is desired to draw current to a negative source, it will be necessary to balance the load by drawing on equal current to a positive source.

ELECTRICAL SPECIFICATIONS

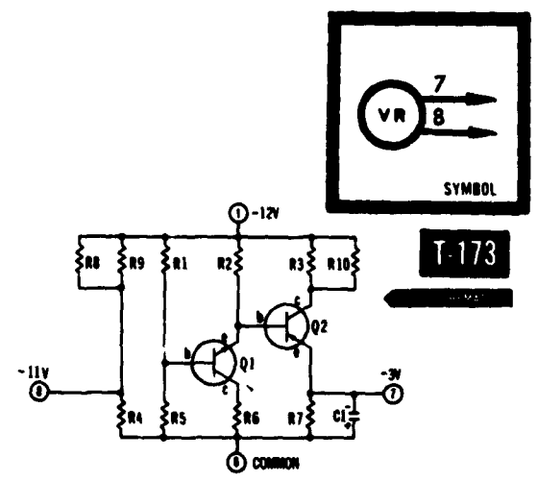
OUTPUT:

Amplitude: −3VDC (±0.3V) at Pin 7 and −11VDC (±0.5V) at Pin 8.

Loading: −3VDC output: 90 ma maximum
−11VDC output: 20 ma maximum

POWER REQUIRED: −12VDC ±10% at 275 ma

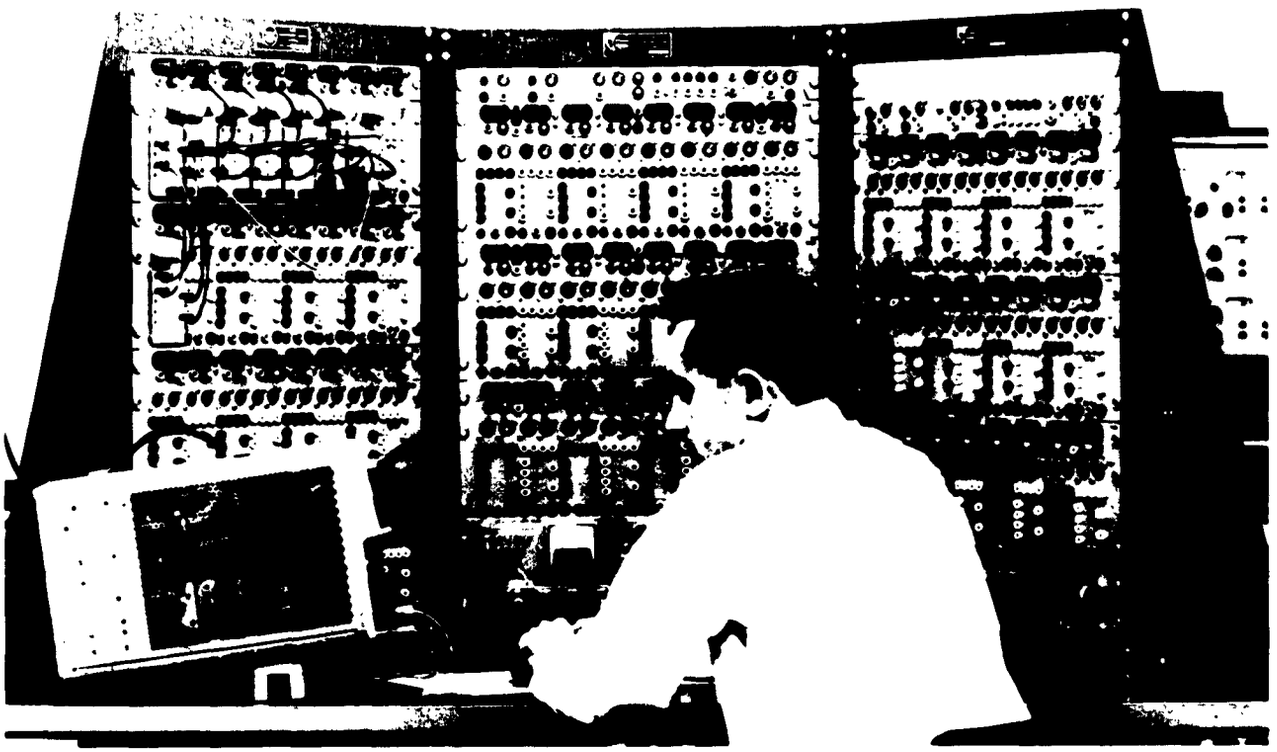
OPERATING TEMPERATURE RANGE: −54 to +71°C



T series related equipment section

This section of the catalog presents information on related equipment which can be used with T and CT-Series circuit modules. This includes:

SEE OUR SPECIFICATIONS IN VSMF THE MICROFILM CATALOG FILE

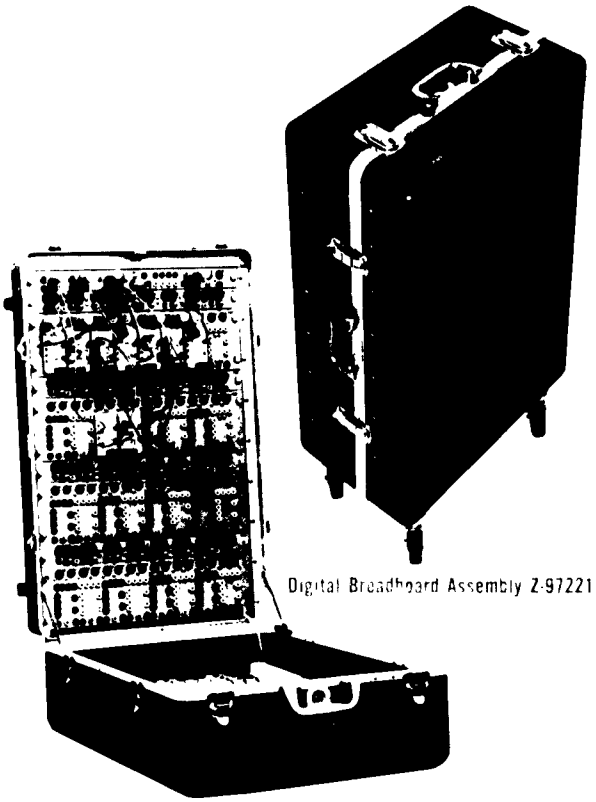


DIGITAL SYSTEM BREADBOARD AND TRAINING EQUIPMENT

This equipment provides a means of rapidly building and testing alternate ways of formulating digital electronic systems or portions of a system. T-Series units to be tried are plugged into sockets on panels. These sockets are permanently wired to groupings of banana jacks immediately underneath the sockets. Plastic circuit symbol cards for each unit type showing circuit symbols, input and output connections, etc., fit over the group of banana jacks exposing the proper pattern for the unit to be connected in the system. Signal connections are then made by patching card-to-card in the line-up being tried. No soldering is necessary (saving engineering time and breadboard materials) and the symbol cards provide means for rapidly visualizing the system or drawing a system diagram.

This equipment can be built up in stages to any desired degree of complexity and the system may be operated slowly to permit detailed observation of each mode of operation. Indicator panels provide light indications, where desired, to show circuit states and, thus, a minimum of external test equipment is required. This equipment is available in either a rack-mounted version (H-180) or a suitcase-mounted portable version (H-181). Because the complement of T-Series units and number and kind of accessories required varies for different users, these equipments are quoted in terms of dash numbers. For example, H-180-1 may contain things that are not necessarily in H-180-2 and vice versa. The purpose of these dash numbers is to allow the large number of items which can make up a given kit to be purchased under just one part number and, thus, minimize purchase order paperwork.

When you have a requirement for a digital system breadboard kit, contact either your local EECo representative or the applications engineers at our factory. These people will work with you to establish your needs and then specify the complement you require and assign a dash number which defines your kit. The following paragraphs identify components of the suitcase-mounted and rack-mounted equipments.



Digital Breadboard Assembly Z-97221

SUITCASE-MOUNTED EQUIPMENT (H-181)

Digital Breadboard Kit H-181 is composed of digital bread-board assembly Z-97221 plus selected T-, N-, U-, and M-Series circuits and circuit cards. Digital bread-board assmbly Z-97221 is an integrated system of bread-boarding panels for systems made up of digital circuit modules. The assembly is contained in a EECo case mounted on casters for ease of portability and includes patch panels, indicator panels, a signal generator panel, power supplies, and storage facilities for plug-in circuits, patch cords, and accessories. The assembly may be used in any location where 115VAC is available; and, since auxiliary test equipment is not ordinarily required, the H-181 is a self-sufficient portable design laboratory. The unit can be locked and stored when not in use.

ELECTRICAL SPECIFICATIONS

Input Power: 115VAC ±10%, 60 cps; maximum of 30 watts. Line frequency may be 50-400 cps if −100VDC or +100VDC power supplies are not operated. Line cord is approximately 15 feet long and has a standard 2-prong plug.

Capacity: The assembly includes 4 T-927 circuit bread-board panels, each of which can accommodate up to eight circuit modules. Thus, this assembly can be used to breadboard systems of up to 32 modules. (H-159 adaptors are necessary to use N-Series modules.)

Supply Voltages Available: Power supply panel Z-97432 provides regulated power for use with any standard T-Series, N-Series, M-Series UB-Series, or R-Series unit. Voltages from this power panel are cabled into the circuit breadboard panels via assembly cabling and are also available for test purposes or external patching purposes at jacks on the power panel.

Voltages available are:

+12VDC, 1 amp
−12VDC, 1 amp
+150VDC, 15 ma (optional)
−100VDC, 15 ma (optional)
−7.5VDC, 18 ma (optional)
−3VDC, 90 ma max. to a positive source
−11VDC, 90 ma max. to a positive source

PHYSICAL SPECIFICATIONS

Dimensions: Aprroximately 36" high x 23" wide x 12" thick.

Weight: Approximately 80 pounds including plug-in circuits and accessories.

Material and Finish: Dark blue Fiberglas with brushed aluminum and chrome plated fittings.

Casters: Four rubber-tired casters, permanently mounted.

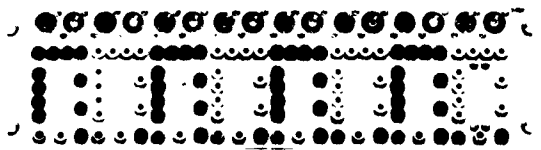
EQUIPMENT INCLUDED IN Z-97221

T-918 and T-958 Indicator and Tie Point Panels (2 Each) 1¾" x 19", with 8 Minisig indicators and 8 dual binding posts for external parts such as resistors, diodes, capacitors, etc. Indicators light when input signal is −3 volts. T-918 accommodates R-341 indicators; T-958 accommodates R-342 indicators. (R-341 draws power mainly from −12 volts and R-342 draws power mainly from +12 volts.)

T-918 Indicator and Tie Point Panel

T-958 Indicator and Tie Point Panel

T-927 Systems Development Panel (4 Supplied) 5¼" x 19", with eight 9-pin and eight 13-pin sockets. Each panel accepts up to 8 circuits at one time. H-159 socket adaptor is necessary for use with N-Series modules. Power connections are permanently wired to the sockets and other circuit conections are wired to the banana jack grouping immediately below the sockets.



T-927 Systems Development Panel

T-965A Signal Generator Panel (1 Supplied less plug-ins) 1¾" x 19" with:

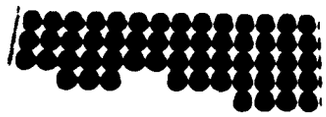
a. 8 toggle switches for manual insertion of data bits.
b. 8 Minisig indicators to show settings of these toggle switches.
c. Socket for T-104 and 5-position rotary selector switch for generation of timing waveform.
d. 2 Minisig indicators to show state of this timing waveform.
e. Push-button switch for DC reset signal.
f. Push-button switch and socket for T-5089 One-shot MV for generation of single clock pulses.

T-965A Signal Generator Panel

related equipment

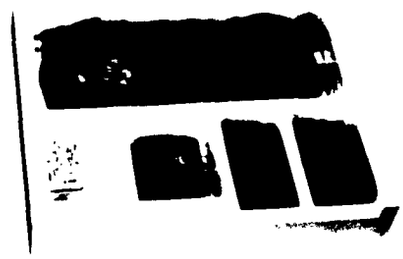
Storage Boxes

The T-946 circuit storage box provides shock resistant storage for up to 96 T-Series circuits. The T-947 accessory storage box is a partitioned container for storing circuit cards, patch cords, component plugs, etc.



T-946 Circuit Storage Box

T-947
Accessory Storage Box

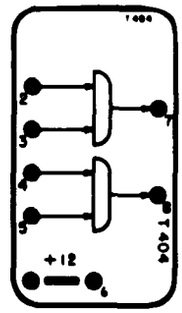


ACCESSORIES (Not included in Z-97221)

Plastic Circuit Symbol Cards

Plastic cards corresponding to specific T-Series circuit modules are imprinted with circuit symbols showing input and output connections, power connections, part numbers, etc.

Perforations in the circuit cards match with banana jacks on the T-927 circuit panels. These cards facilitate patching circuit interconnections, visualizing the system, drawing a system diagram, and determining the cost of a system. Circuit cards are available as T-919/xxx, where xxx is the appropriate circuit number. For example: T-919/101B is a circuit card for flip-flop T-101B.



Typical Plastic Circuit Symbol Card

Patch Cords

Patch cords H-106 through H-120 are available in 8", 12", and 18" lengths, and in black, red, green, blue, and yellow, to facilitate circuit interconnection identification. Black patch cords are also available in 4" lengths as H-101. (For specific part numbers see Price List.)

Power Plugs

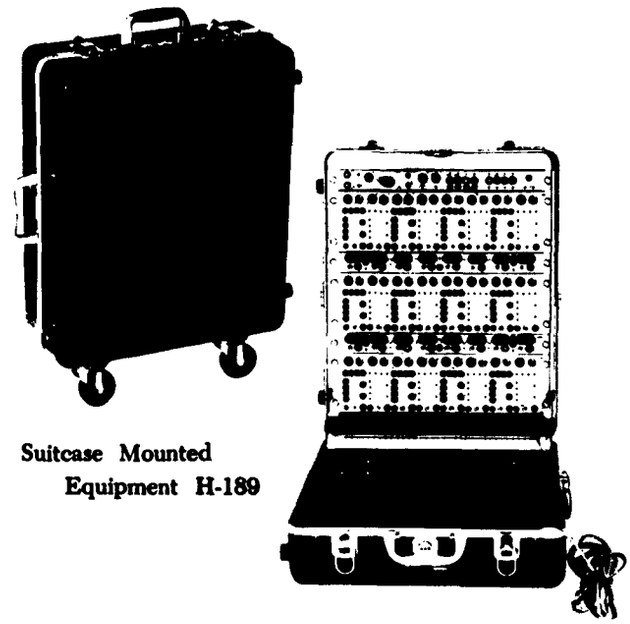
T-920 power plugs are black dual banana plugs with a shorting bar between pins. These are used to make +12 volt and ground connections on T-927 panels.

Component Plugs

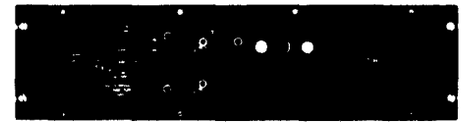
Component plugs are available in red (T-928), yellow (T-929), and blue (T-930). These are similar to the T-920 power plug but do not have a shorting bar. Component plugs are used with the T-918 and T-958 panels to hold a resistor, capacitor, or diode, and are mounted between dual binding posts.

SUITCASE MOUNTED EQUIPMENT (H-189)

Digital Breadboard Kit H-189 is a smaller version of Kit H-181. The case contains a T-965A Signal Generator Panel, 3 T-927 System Development Panels, 2 T-958 Indicator and Tie-Point Panels, and a Z-101663 Power Panel Specific kits also contain selected T-, N-, and UB-Series circuit modules and accessories; dash numbers are assigned, as previously described, to define each specific kit.



Suitcase Mounted Equipment H-189



Power Panel Z-101663

ELECTRICAL SPECIFICATIONS

Input Power: 115VAC ±10%, 50 to 400 cps. Maximum power drain is 30 watts. Line cord is 15 feet long and has standard 2-prong plug.

Capability: The assembly includes 3 T-927 circuit breadboard panels, each of which can accommodate up to eight digital modules. Thus, systems of up to 24 modules can be handled.

Supply Voltages Available: Power Panel Z-101663 provides regulated power for use with any standard T-, N-, and UB-Series units. Voltages from this Power Panel are coupled to the circuit breadboard panels via assembly cabling and are also available for test purposes or for external patching purposes at jacks on the power panel.

Voltages Available Are:

+12VDC	−6VDC
−12VDC	−3VDC
+6VDC	−11VDC

PHYSICAL SPECIFICATIONS

Dimensions: Approximately 24" high x 20" wide x 9" thick.

Weight: Approximately 40 lbs. including plug-ins and accessories.

Material and Finish: Dark blue Fiberglas with brushed aluminum and chrome plated fittings.

Casters: Four rubber-tired casters, permanently mounted.

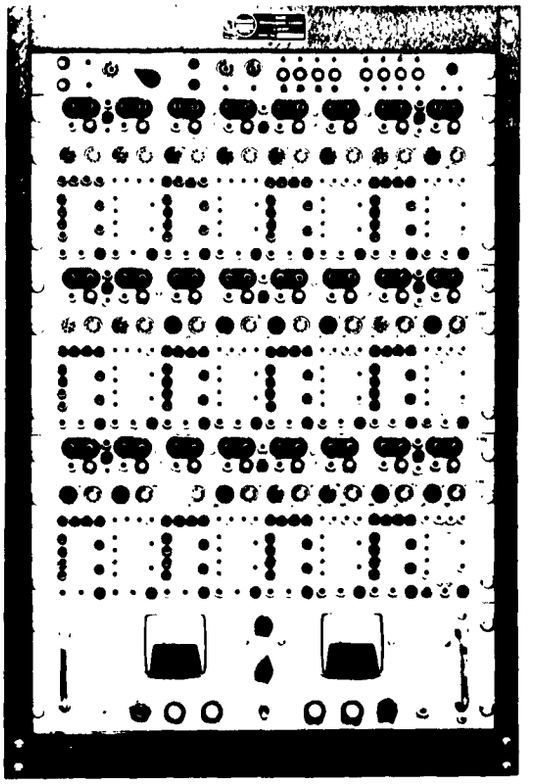
RACK-MOUNTED EQUIPMENT (H-180)

Rack-Mounted Digital Breadboard Kits H-180 are comprised of rack-mounted assemblies Z-97597A, Z-97598, and Z-97599A plus the accessories described for digital breadboard Kit H-181. The rack-mounted digital breadboard assemblies form an integrated system of breadboarding panels for circuits made up of EECo digital modules. These assemblies are mounted in racks for laboratory or classroom use and include: Power supplies, breadboarding panels, indicator panels, signal generator panel, and system cabling.

Each assembly is intended primarily for experimental breadboarding of portions of larger digital systems. Combinations of assemblies may be used to breadboard complete digital systems and such combinations are designated a Digital Breadboard Kit H-180. Dash numbers can then be appended to the part number (H-180-1, H-180-2, etc.) in order to define each specific kit.

Z-97597A includes a dual 5-amp power supply ZA-720 and a signal generator panel T-965A. In applications where more than 24 plug-ins are required, Z-97597A can be used to provide power and signals to one or more Z-97598 assemblies which contain only breadboarding and indicator panels. If 24 or less plug-ins are required, a Z-97599A assembly can be used. Accessory equipment for these assemblies is the same as described for the suitcase mounted Kit H-181. Circuit and accessory storage boxes may be purchased separately.

The following paragraphs briefly describe these three rack-mounted digital assemblies.



Z-97597A

This rack forms a nucleus of several breadboard assemblies made up of the Z-97597A and one or more Z-97598 auxiliary assemblies. Inter-rack cabling feeds power from Z-97597A to the companion Z-97598 assemblies. In addition to the power supply, Z-97597A contains a T-965A signal generator panel, one T-918 and two T-958 indicator and tie point panels, and three T-927 system development panels.

PHYSICAL SPECIFICATIONS

Dimensions: Approximately 32" high x 21" wide x 17" deep.

Finish: Rack is gray wrinkle; panels are gray baked enamel.

ELECTRICAL SPECIFICATIONS

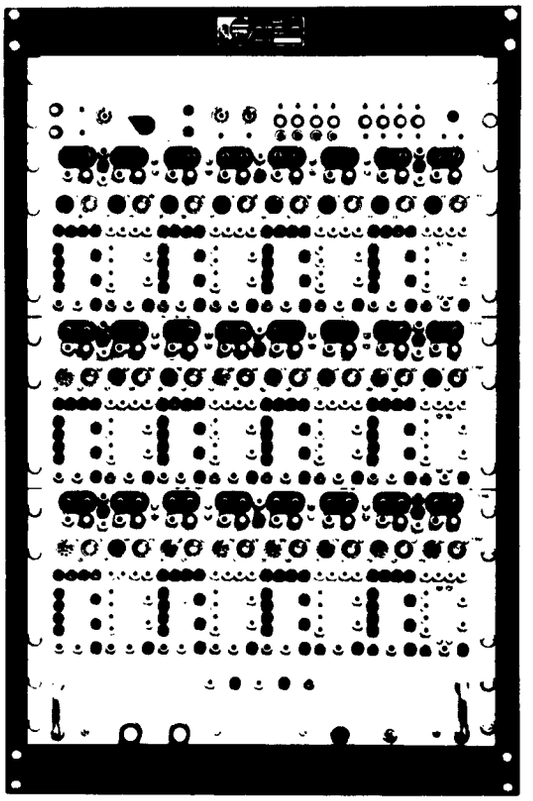
Input Power: 115VAC, 50-400 cps, 120 watts maximum. Power cord is 8 feet long and has a standard two-prong plug.

Circuit Breadboarding Capability: Assembly includes three T-927 system development panels, each of which can accommodate up to eight modules at one time.

Output Power Capability: Power supply provides two channels of regulated 12-volt power. Each channel is rated at 5 amperes. Power is terminated at a terminal board on the rack and inter-rack cabling must be used to carry power to other racks in the system.

continued on next page

related equipment



Z-97599A

This assembly is intended primarily for experimental breadboarding of portions of larger digital systems. The assembly contains a T-965A signal generator panel, a T-918 and two T-958 indicator and tie point panels, a Z-97617 panel/chassis power supply, and three T-927 system development panels.

PHYSICAL SPECIFICATIONS

Dimensions: Approximately 32" high x 21" wide x 15" deep.

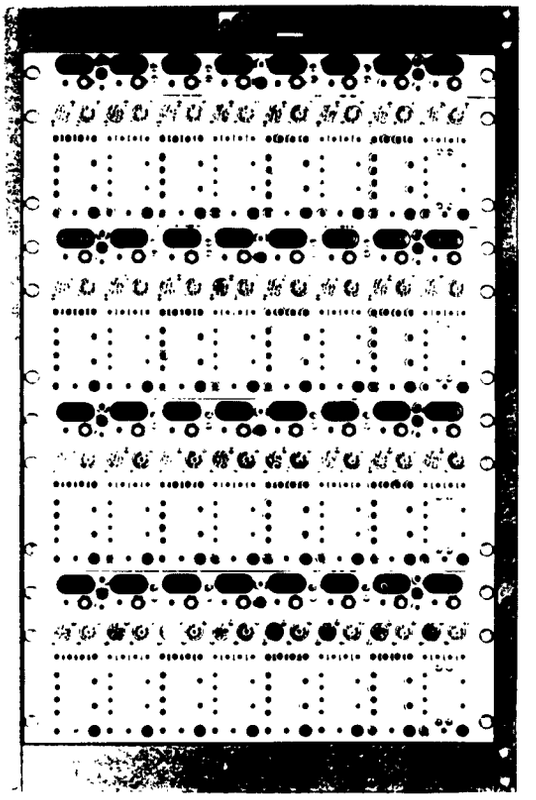
Finish: Rack is gray wrinkle; panels are gray baked enamel.

ELECTRICAL SPECIFICATIONS

Input Power: 115VAC ±10%, 50-400 cps. Maximum power drain is 25 watts. AC line cord is 8 feet long and has standard 2-prong plug.

Circuit Breadboarding Capability: Assembly includes three T-927 system development panels. Each panel accommodates up to eight modules; a total capacity of 24 modules at one time.

Power Supply Voltages: Z-97617 panel/chassis power supply provides −12VDC, +12VDC, −11VDC, and −3VDC. Power supply voltages are cabled to system development panels by a rack cabling. Power supply voltages are also available at test jacks on the Z-97617 panel.



Z-97598

This is a companion unit for Z-97597A and is used in layout of extensive breadboarding facilities for digital modules. This assembly contains T-927 development panels and T-918 and T-958 indicator panels only. Power must be supplied from either the Z-97597A or from external power supplies.

PHYSICAL SPECIFICATIONS

Dimensions: Approximately 32" high x 21" wide x 15" deep.

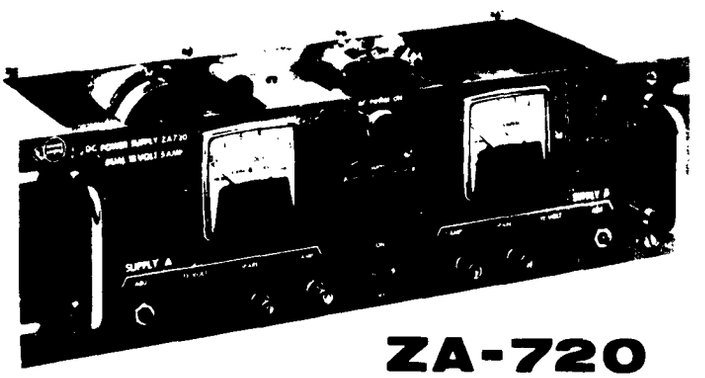
Finish: Rack is gray wrinkle; panels are gray baked enamel.

ELECTRICAL SPECIFICATIONS

Input Power: +12VDC and −12VDC. Input power is supplied to the terminal board on the rack.

Circuit Breadboarding Capability: The system includes four T-927 system development panels. Each panel can accommodate up to eight modules at one time

These units can function as power sources for transistorized systems and equipment employing EECo T-Series or CT-Series Digital Circuit Modules, N-Series Plug-In Decade Counters, R-Series Minisig® Indicators, U-Series NOR circuits, and M-Series Magnetic Core-Transistor Circuit Modules as well as for Digital System Breadboard and Training Equipment. These supplies can be used effectively in the laboratory or for integration into complex systems.



ZA-720

Model ZA-720 is a solid-state, convection-cooled, dual 12-volt DC, 5-amp regulated power supply featuring military-quality parts and excellent regulation. Ripple voltage is held to less than 0.001 volt rms under the worst combination of input voltage and load current.

The supply provides two completely independent 12-volt DC sources, rated at 5-amps each, isolated from ground and from the chassis. Either polarity may be grounded or the two source outputs may be placed in series. Operating temperature range is −20°C to +65°C (−4°F to +149°F).

Two meters on the front panel permit measurement of output voltage and current for each supply independently. A switch is provided for selection of source to be measured.

ELECTRICAL SPECIFICATIONS

Input Power: 115V (±10%) AC, 2 amps, 50-400 cps.

Output Power: Supply A: 12VDC at 0-5 amps.

Supply B: 12VDC at 0-5 amps.

(Either polarity may be grounded, or both may be placed in series.)

Both supplies are independently adjustable over the range of 11 to 13V.

Regulation:

Voltage Regulation: 0.1% at DC to 1% at 25Kc for any load change between 0 and 5 amps, and/or any input voltage specified.

Ripple Voltage: Less than 0.001 volt rms under the worst combination of input voltage and load current.

Output Impedance: Figure 1 shows a typical variation of output impedance over the frequency range of 10 cps to 1Mc. Below 10 cps the impedance is still lower and falls to a typical value of 0.001Ω at DC.

Duty: Continuous.

PHYSICAL SPECIFICATIONS

Mounting: Standard rack-panel mounting with amateur notching. Chassis sliders optional.

Weight: 35 pounds.

Dimensions: 5¼" panel height, 19" width, 14" depth behind panel.

Finish: Panel is finished in gray enamel; chassis is cadmium-plated steel, clear iridite.

Front Panel Controls:

Meters: The output voltage and current are measured by two meters on the front panel. The supply to be measured is selected by a switch located between the two meters.

Output Voltage Control: Output voltage of either supply may be varied ±1VDC by adjusting its individual potentiometer mounted on the front panel.

Fuzes: One 2.0-amp fuze and one spare for each supply.

Front Panel Indicators:

Power on (red).
DC power on (amber).
Blown-fuze indicators.

Cooling: Convection.

Operating Temperature Range: −20°C to +65°C (−4°F to +149°F). May be operated at +71°C if maximum load current is reduced to 4 amps.

Pin Connections:

Terminal 1 (TB1 and TB2): 115VDC input.
Terminals 3 and 4: (TB1 and TB2): negative output terminal.
Terminal 5: (TB1 and TB2): chassis ground.
Terminals 6 and 7: (TB1 and TB2): positive output terminal.

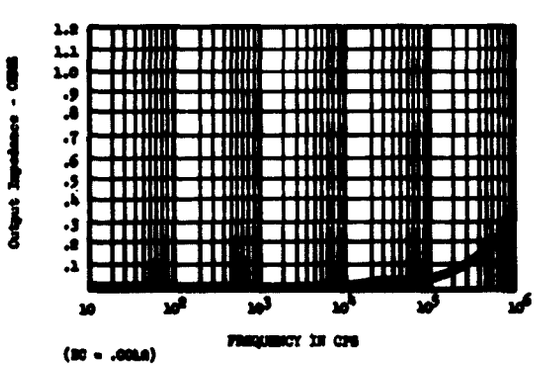
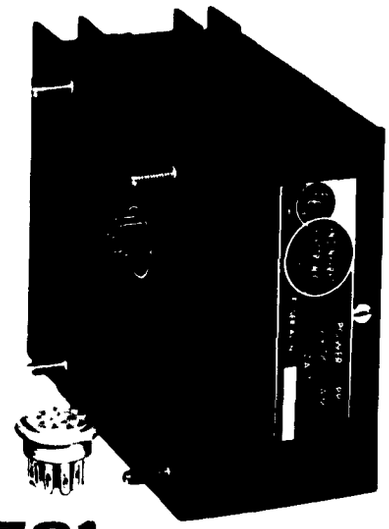
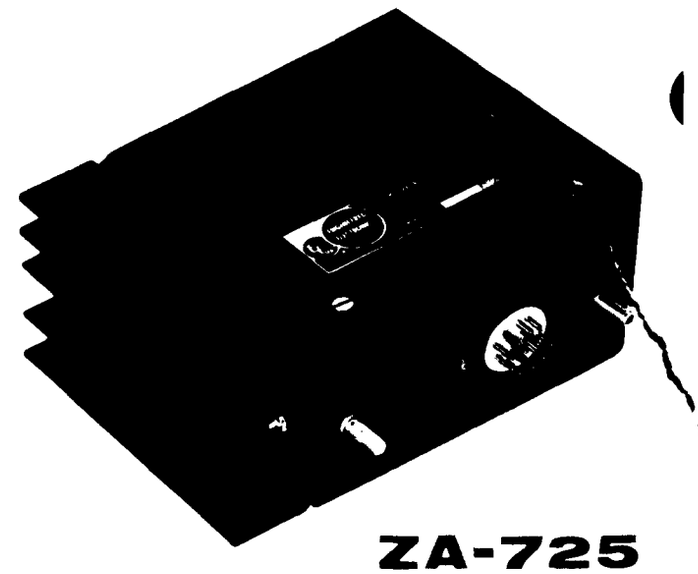


Fig. 1 Output Impedance vs Frequency ZA-720



ZA-721



ZA-725

Models ZA-721 and ZA-725 are plug-in, solid-state, convection-cooled, 12-volt DC, 1-amp regulated power supplies featuring military-quality parts and excellent regulation. Ripple voltage is held to less than 0.001 volt rms under the worst combination of input voltage and load current.

The supplies are isolated from the chassis and can be used as either positive or negative voltage sources with reference to ground. Operating temperative range is −20°C to +65°C (−4°F to +149°F).

Attractively finished in black anodize, the units weigh only 2-1/2 pounds and can be mounted on a chassis along with other circuitry. Four #8-32 x 7/16" studs secure ZA-721 supply to a mounting surface; two #8-32 x 7/16" studs secure the ZA-725 to a mounting surface. Both units plug into a modified 14-pin miniature relay-type socket.

ELECTRICAL SPECIFICATIONS

Input Power: 115V (±10%) AC, 0.3 amp, 50-400 cps.

Output Power: 12VDC, 0-1 amp (+ or −), adjustable over the range of 11 to 13V (33VAC with center tap at positive terminal available for auxiliary positive bias unit).

Regulation:

Voltage: 0.16% at DC to 1% at 25Kc for any load change between 0 and 1 amp and/or for any input voltage specified. This includes an output connector loss of 0.12%.

Ripple: Less than 0.001 volt rms under the worst combination of input voltage and load current.

Output Impedance: See Figure 1 which shows a typical variation of output impedance over the frequency range of 10 cps to 1Mc. Below 10 cps the impedance is still lower and falls to a typical value of 0.02 at DC.

Duty: Continuous.

PHYSICAL SPECIFICATIONS

Mounting: Models ZA-721 and ZA-725 power supplies can be mounted on a chassis along with other circuitry. They plug into modified 14-pin miniature sockets which are furnished with the unit. Four studs secure the ZA-721 to a mounting surface; two studs secure the ZA-725 to a mounting surface.

Weight: 2-1/2 pounds.

Dimensions: 3-3/4" x 4-3/4" x 2-3/16".

Seated Height:
ZA-721 — 2-3/16"
ZA-725 — 3-3/4"

Finish: Black anodize.

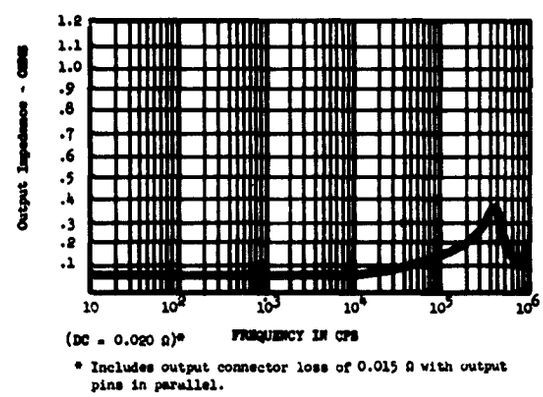
Output Voltage Control: Output voltage may be varied over the range of 11 to 13VDC to adjusting a potentiometer through opening in the heat-sink side of the power supply.

Fuzes: ½-amp fuze should be used external to this unit in series with the AC input power line. ¾-amp slo-blo fuze is used within the unit to prevent damage in the event of faulty external fuzing.

Cooling: Convection.

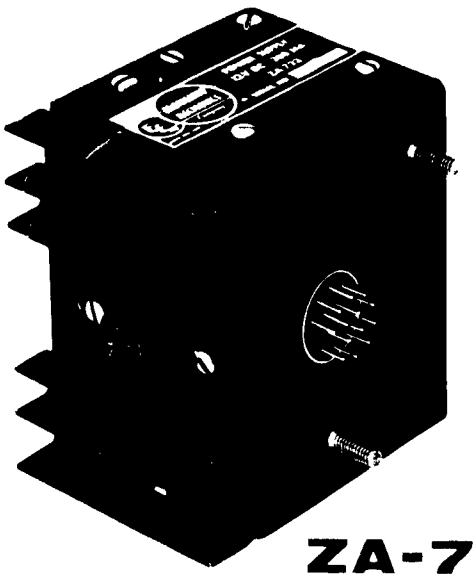
Operating Temperature Range: −20°C to +65°C (−4°F to +149°F)

Pin Connections:
Pins 4 and 12: Input 115VAC at 0.3 amp (external ½-amp fuze required).
Pins 1 and 2: Output negative terminal.
Pins 6 and 7: Output positive terminal.
Pins 8 and 9: 33VAC center tapped at Pins 6 and 7.
Pins 3, 5, 11, 13, and 14: Case common (connect to chassis ground).



* Includes output connector loss of 0.015 Ω with output pins in parallel.

Fig. 1 Output Impedance vs Frequency



ZA-723

Model ZA-723 is a plug-in, solid-state, convection-cooled, 12 volt DC, 300 ma regulated power supply featuring military-quality parts and excellent regulation. Ripple voltage is held to less than 0.001 volt rms under the worst combination of input voltage and load current.
The supply is isolated from the chassis and can be used as either a positive or negative voltage source with reference to ground. Operating temperature range is −20°C to +65°C (−4°F to +149°F).

Attractively finished in black anodize, the unit weighs only 1¾ pounds and can be mounted on a chassis along with other circuitry. Two #8-32 x ½" studs secure the supply to the mounting surface.

ELECTRICAL SPECIFICATIONS

Input Power: 115 (±10%) volts AC, 0.1 ampere, 50-400 cps.

Output Power: 12VDC, 0-0.3 amp (+ or −), adjustable over the range of 11 to 13V (33VAC with center tap at positive terminal available for auxiliary positive bias unit.

Regulation:

Voltage: 0.1% at DC to 1% at 25Kc for any load change between 0 and 0.3 amp and/or for any input voltage specified. This includes an output connector loss of 0.05%.

Ripple: Less than 0.001 volt rms under the worst combination of input voltage and load current.

Output Impedance: See Figure 1 which shows a typical variation of output impedance over the frequency range of 10 cps to 1Mc. Below 10 cps, the impedance is still lower and falls to a typical value of 0.04Ω at DC.

Duty: Continuous.

PHYSICAL SPECIFICATIONS

Mounting: Model ZA-723 power supply can be mounted on a chassis along with other circuitry. It plugs into a modified 14-pin miniature socket which is furnished with the unit. Two #8-32 x 1/2" studs secure this supply to a mounting surface.

Weight: 1-3/8 pounds.

Dimensions: 2-7/8" x 2-7/8" x 2-3/16" seated height.

Finish: Black anodize.

Output Voltage Control: Output voltage may be varied over the range of 11 to 13VDC by adjusting a potentiometer through opening in the heat-sink side of the power supply.

Fuzes: A 1/4-amp fuze should be used external to this unit in series with the AC input power line. 3/8-amp slo-blo fuze internal to supply to prevent damage in the event of faulty external fuzing.

Cooling: Convection.

Operating Temperature Range: −20°C to +65°C (−4°F to +149°F).

Pin Connections: Pin hole No. 10 is blocked in the socket and Pin No. 10 is deleted from the header to provide pins 6 and 7.
index keying. Pin connections are as follows:
Pins 4 and 12: Input 115VAC power at 0.1 ampere.
Pins 1 and 2: Output negative terminal.
Pins 6 and 7: Output positive terminal.
Pins 8 and 9: Output 33 volt AC, center-tapped at pins 6 and 7.
Pins 3, 5, 11, 13, and 14: Case Common (connect chassis ground).

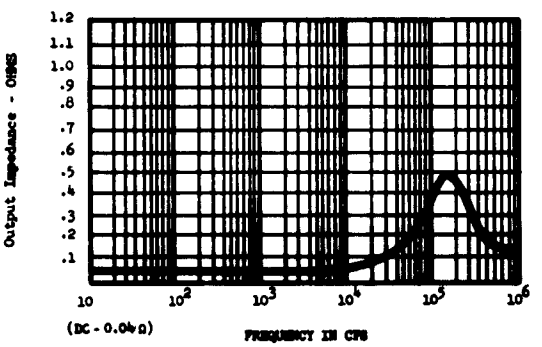
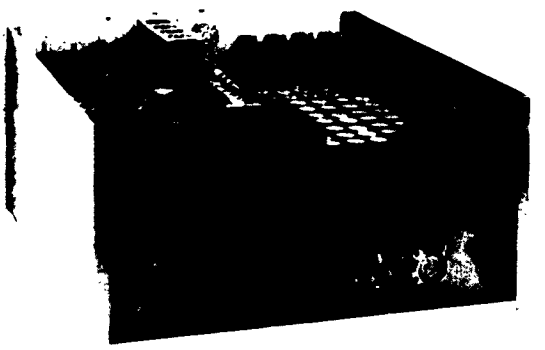
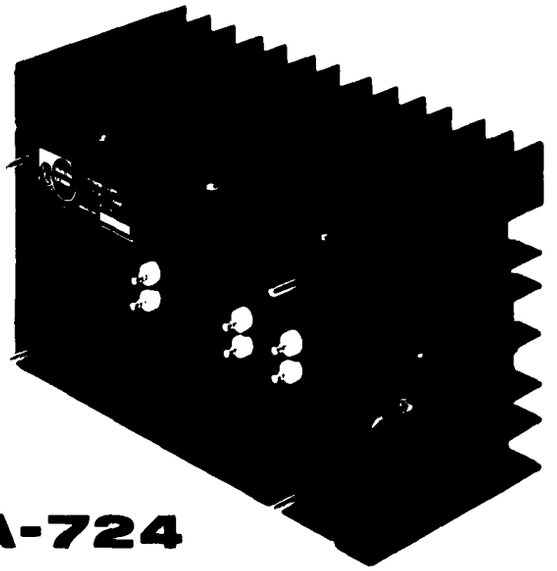


Fig. 1 Output Impedance vs Frequency ZA-723



Example of use of one ZA-724 and one ZA-725 on 2 chassis.



ZA-724

Power Supply ZA-724 is a general-purpose, transistorized, regulated power supply that will provide 12 volts DC to a 3-amp load in continuous-duty operation. AC and DC circuits are isolated from the case, and either output terminal may be grounded to provide a positive or negative output with respect to circuit ground. The unit may be secured to a chassis by means of four #8-32 x ½" studs that are integral with the case. Electrical connections are made to feed-through terminals on the bottom of the case. Attractively finished in black anodize, the unit weighs only 6 pounds and can be mounted on a chassis along with other circuitry. The seated height is 3¾".

ELECTRICAL SPECIFICATIONS

Input Power: 115 (±10%) volts AC, 1 ampere, 50-400 cps.

Output Power: 12 volts DC, 0-3 amp (+ or −), adjustable over the range of 11 to 13 volts. (33 volts AC with center tap at positive terminal available for auxiliary positive bias unit).

Regulation:

Voltage Regulation: 0.1% at DC to 1% at 25Kc for any load change between 0 and 3 amp and/or for any input voltage specified.

Ripple: Less than 0.001 volt rms under the worst combination of input voltage and load current.

Output Impedance: See Figure 1 which shows a typical variation of output impedance over the frequency range of 10 cps to 1Mc. Below 10 cps the impedance is still lower and falls to a typical value of 0.004Ω at DC.

PHYSICAL SPECIFICATIONS

Mounting: The power supply can be mounted on a chassis along with other circuitry. Feed-through type input and output terminals are on the bottom of the supply; these terminals fit through 3 holes, ¾" diameter in the chassis. Both input and output power connections are soldered connections.

Weight: 6 pounds.

Dimensions: 7⅞" x 4¾" x 3¾" seated height.

Finish: Black anodize.

Output Voltage Control: Output voltage may be varied over the range of 11 to 13 volts DC by adjusting a potentiometer through an opening in the back of the power supply.

Fuze: A 1½-ampere fuze is internal to the supply and is accessible from a screw-driver-operated fuze extractor in the top of the power supply.

Cooling: Convection.

Operating Temperature Range: −20°C to +65°C (−4°F to +149°F).

Pin Connections:

Pins 1 and 2: Input 115 volts AC power at 1 ampere.
Pin 5: Negative output terminal.
Pin 6: Positive output terminal.
Pins 3 and 4: 33 volt AC output, center tapped at Pin 6.
Pins 8 and 9: Output positive terminal.

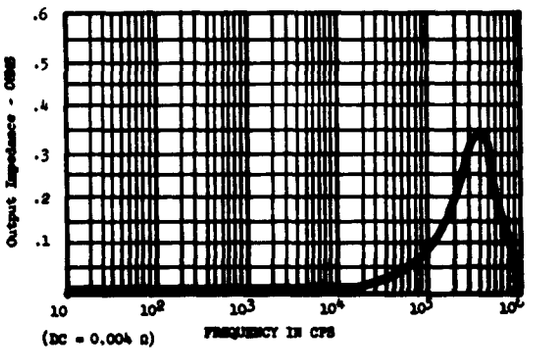
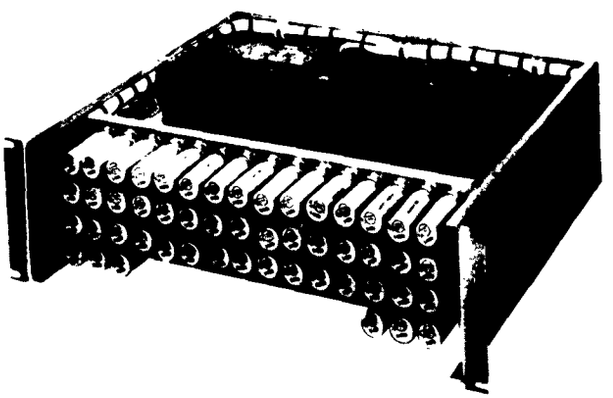
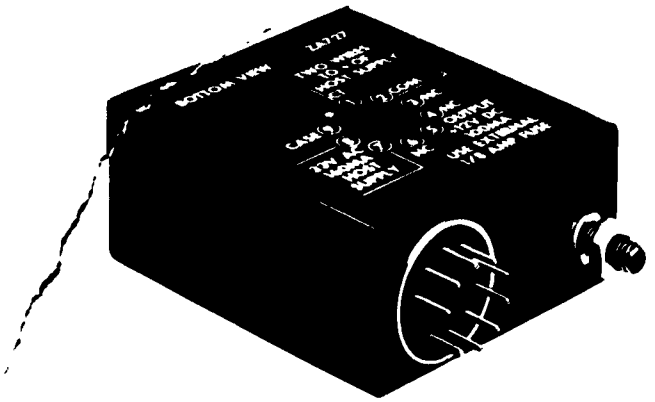


Fig. 1 Output Impedance vs Frequency ZA-724



Example of use of two ZA-724 power supply on a chassis.



ZA-727

Bias Supply ZA-727 is an auxiliary regulated power supply that will furnish +12 volts DC or +24 volts DC to a 100-milliampere load in continuous-duty operation. Input power is provided by another (host) power supply. The unit features military-quality parts and excellent regulation. Ripple voltage is held to less than 0.001 volt rms under the worst combination of the input voltage and load current. Host supplies can be ZA-721, ZA-725, ZA-723+, or ZA-724.

+When Model ZA-727 is used to furnish full 100-ma bias current, derate Model ZA-723 to 250 ma.

Attractively finished in black anodize, the unit weighs only 2 ounces and can be mounted on a chassis along with other circuitry. One #8-32 x ½" stud secures the supply to a mounting surface.

ELECTRICAL SPECIFICATIONS

Input Power: 33 volts AC, 160 ma, 50-400 cps from center-tapped transformer secondary of ZA-721, ZA-723, ZA-724, or ZA-725 power supplies.

Output Power: +12 volts DC, 0-100 ma with respect to positive terminal of host supply. The positive terminal of the host power supply is used as a common DC return point.

Regulation:

Voltage Regulation: Less than 0.1% at DC from no load to full load of 100 ma and/or for input variations as specified for operation of host supply.

Ripple: Less than 0.001 volt rms under the worst combination of input voltage and load current.

Output Impedance: See Figure 1 which shows a typical variation of output impedance over the frequency range of 10 cps to 1Mc. Below 10 cps, the impedance is still lower and falls to a typical value of 0.02Ω at DC.

PHYSICAL SPECIFICATIONS

Mounting: The bias supply can be mounted on a chassis along with other circuitry. It plugs into a 9-pin miniature tube socket, which is furnished with the unit. One #8-32 x 1/2" stud secures the supply to a mounting surface.

Weight: 2 ounces.

Dimensions: 1" x 1-13/16" x 2-3/16" seated height.

Finish: Black anodize.

Fuze: Internal 3/10 amp.

Cooling: Convection.

Operating Temperature Range: −20°C to +65°C (−4°F to +149°F).

Pin Connections:

Pins 7 and 8: Input 33 volt AC power at 100 ma from transformer secondary of host supply.

Pin 1: Return to center tap of transformer of host supply.

Pin 5: +12 volt DC output at 100 ma.

Pin 2: Common return to positive terminal of host supply (must be separate wire from that called out on Pin 1 above).

Pin 9: Case ground.

Pins 3, 4, and 6: Not used.

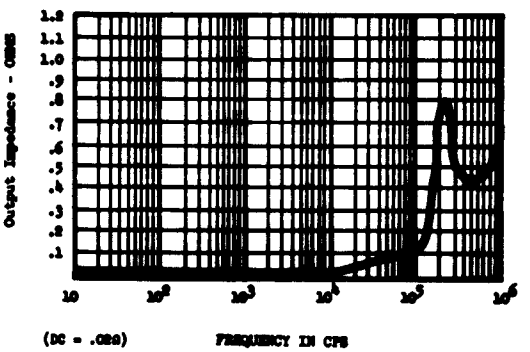
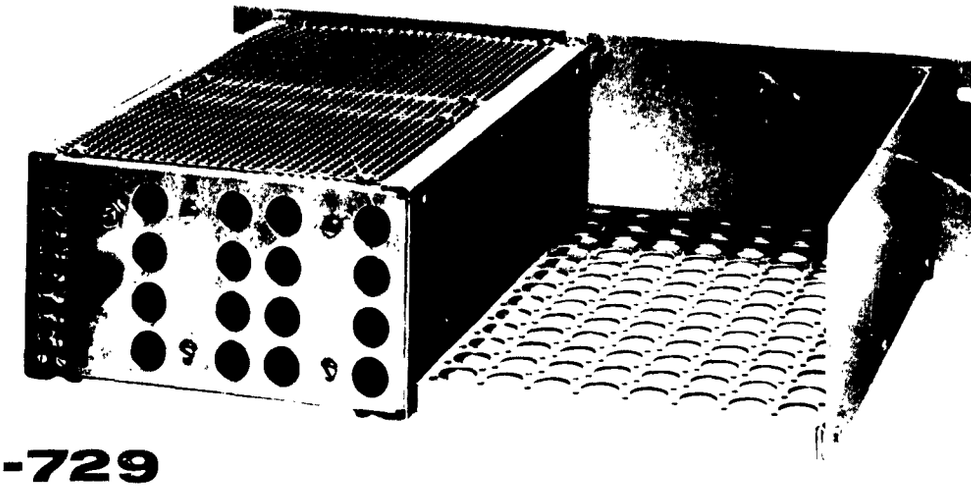


Fig. 1 Output Impedance vs Frequency ZA-727



ZA-729

Model ZA-728 is a general purpose transistorized regulated power supply that will provide 12 volts DC to a 5-ampere load in a continuous-duty operation. AC and DC circuits are isolated from the case, and either output terminal may be grounded to provide a positive or negative output with respect to circuit ground. Model ZA-728 is designed for mounting on a panel. Model ZA-729 consists of a Model ZA-728 power supply mounted on a standard 19" panel (Amateur standard notching) with a chassis and supporting side-brackets; the chassis will accommodate other power supplies or other circuit components. Electrical connections to Models ZA-728 and ZA-729 are made via a Jones barrier strip at the rear of the units.

Both units have front panel finished in gray enamel.

Chassis and side-brackets are cadmium-plated per MIL Spec QQ-P-416, Class 2, Type II.

ELECTRICAL SPECIFICATIONS

Input Power: 115 (±10%) volts AC, 1.5 amperes, 50-400 cps.

Output Power: 12VDC, 0 to 5 amperes (+ or −) adjustable over the range of 11 to 13 volts.

Regulation:

Voltage Regulation: 0.1% at DC to 1% at 25Kc for any load change between 0 and 5 amperes and/or for any input voltage.

Ripple: Less than 0.001 volts rms under the worst combination of input voltage or load current.

Output Impedance: Figure 1 shows the typical variation of output impedance over the frequency range of 10 cps to 1Mc. Below 10 cps the impedance is still lower and falls to a typical value of 0.001Ω at DC.

Duty: Continuous.

PHYSICAL SPECIFICATIONS

Mounting:

ZA-728: Two supplies can be mounted on one 5¼" by 19" panel.

ZA-729: Standard rack panel mounting with 5¼" by 19" panel. Mounting holes for fuzes and input/output cables are located on rear of all auxiliary chassis. The auxiliary chassis will accommodate up to 104 T-Series Plug-Ins or a combination of T-Series and the standard line of 12-volt power supplies.

Weight:

ZA-728 — 18 pounds.
ZA-729 — 19½ pounds.

Dimensions:

ZA-728: 7¾" wide x 4¼" high x 14" deep.
ZA-729: 19" wide x 5¼" high x 14" deep.

Output Voltage Control: Output voltage may be varied for the range of 11 to 13 volts DC by adjusting a potentiometer at the rear of the supply.

Fuze: One 2-ampere fuze at the rear of the supply.

Cooling: Convection.

Operating Temperature Range: −20°C to +65°C (−4°F to +149°F).

Pin Connections:

Pins 1 and 2: 115 volt AC power input.
Pins 3 and 4: Negative output terminal.
Pins 6 and 7: Positive output terminal.
Pin 5: Case common (connect to chassis ground).

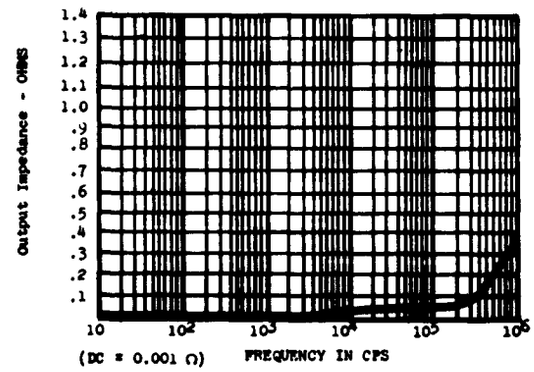
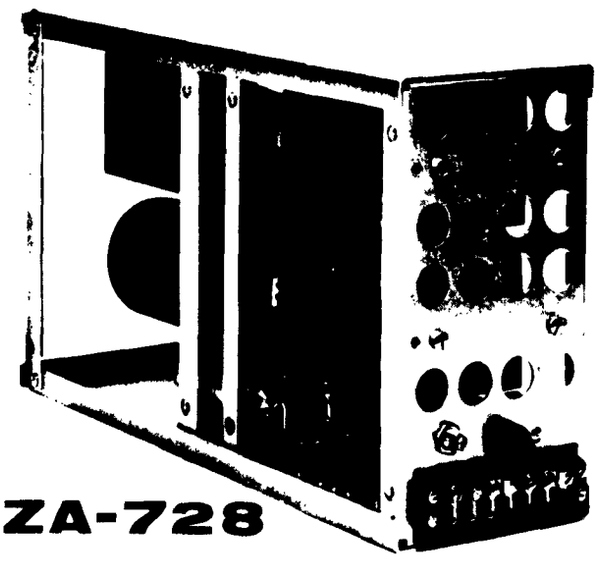
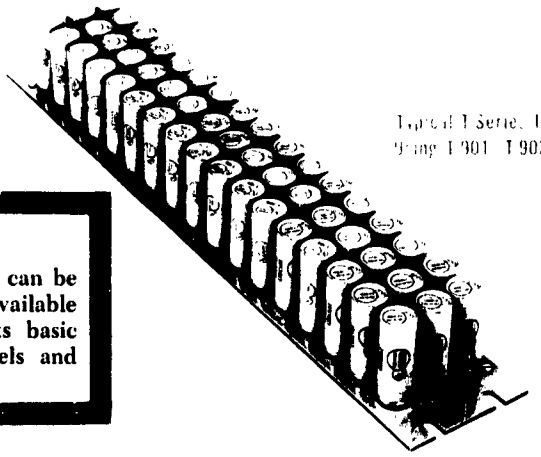


Fig. 1 Output Impedance vs Frequency ZA-728 and ZA-729



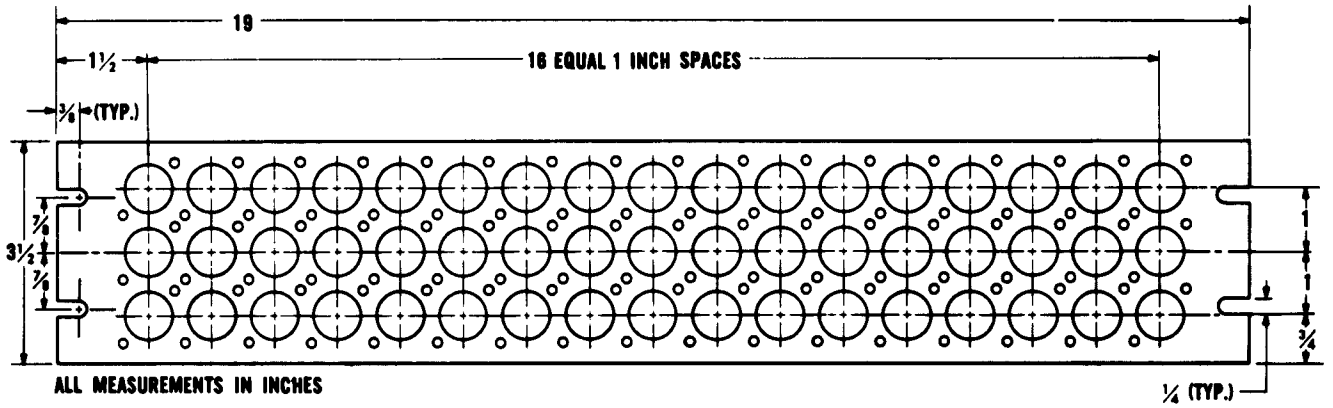
ZA-728



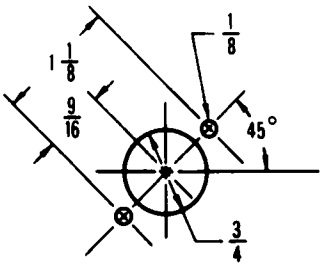
Typical T Series Installation Using T-901, T-902, or T-903

PANELS AND CHASSIS

Several kinds of panels upon which T-Series units can be mounted and two kinds of universal chassis are available from EECo. This section of the catalog presents basic information and outline drawings for these panels and chassis.



Layout of Panels T-901, T-902, T-903



T-901, T-902, and **T-903** are all 3½" x 19" panels which can accommodate up to 51 T-Series circuits. These panels all have a gray finish and standard Amateur notich and holes for sockets are drilled on 1-inch centers. T-901 is supplied without sockets, T-902 is identical but with 9-pin sockets installed, and T-903 is identical to T-902 but with the sockets buss-wired for power.

T-932-1 has the same outline dimensions as T-901 but has only 38 socket holes. These holes are spaced on 1.3-inch centers across the 19-inch dimension and on 1.1-inch centers across the 3½-inch dimension in order to allow room for IERC hold down hardware.

T-932-2 is the same basic panel as T-932-1 with sockets and hold down hardware furnished unassembled. See price list for specific parts.

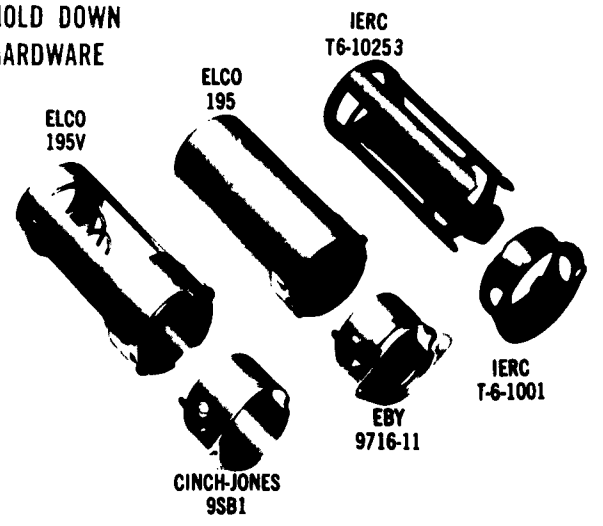
T-933-1 has the same outline dimensions as T-901 but has only 45 socket holes spaced on 1⅛-inch centers to accommodate EBY, Cinch-Jones, and Elco hold down hardware.

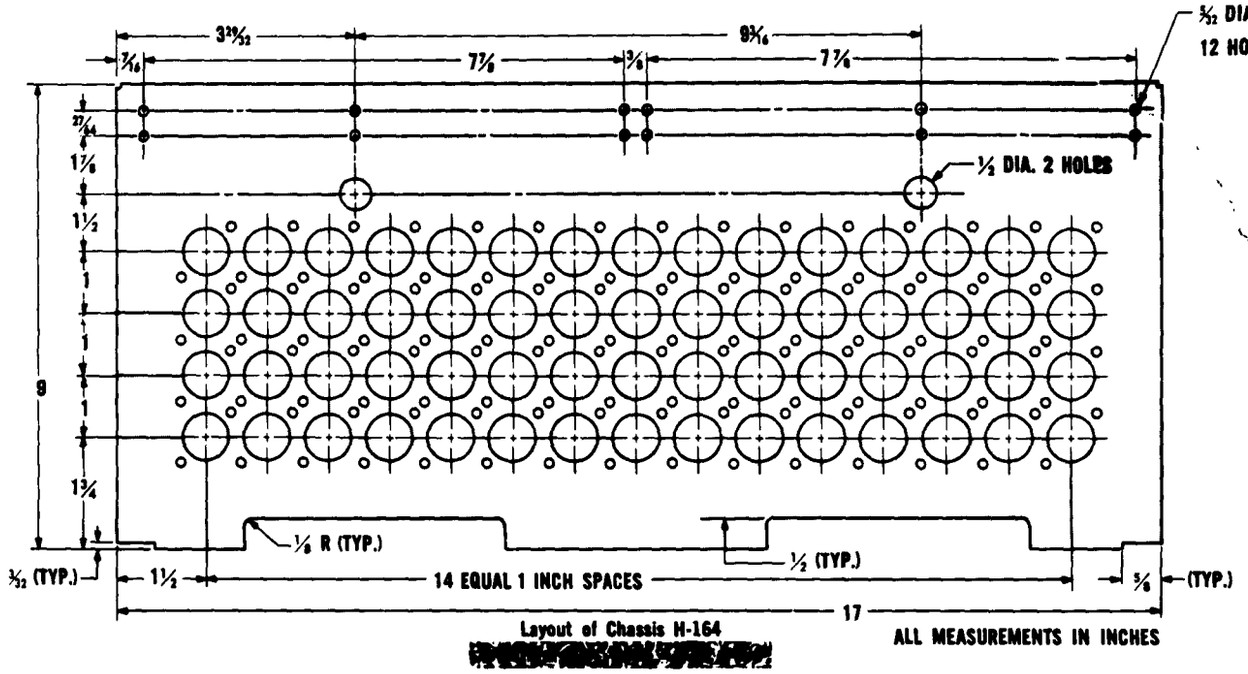
T-933-2 consists of panel T-933-1 and 45 each sockets, bases, and shields furnished unassembled. See price list for specific part numbers.

T-961 is identical to T-902 except 13 pin sockets are installed.

T-962 is identical to T-903 except 13-pin sockets are installed.

HOLD DOWN HARDWARE



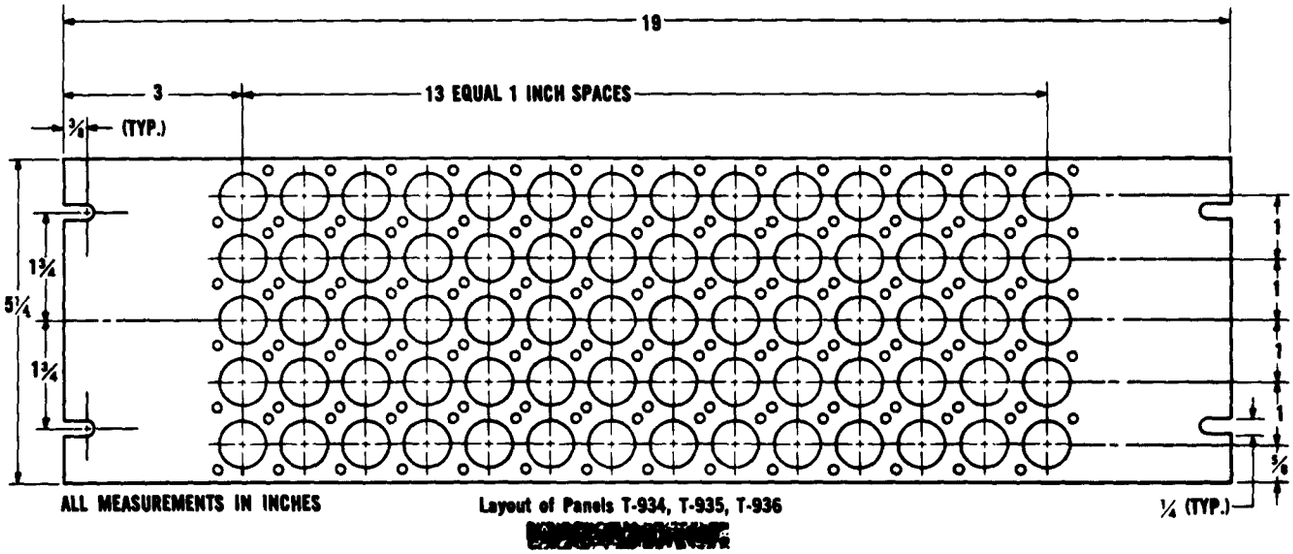


T-934, T-935, and **T-936** are all 5¼" x 19" panels which can accommodate up to 70 T-Series circuits. These panels all have a gray finish and standard Amateur notch and holes for sockets are drilled on 1-inch centers. T-934 is supplied without sockets, T-935 is identical but with 9-pin sockets installed, and T-936 is identical to T-935 but with the sockets buss-wired for power.

T-963 is identical to T-935 expect 13-pin sockets are installed.

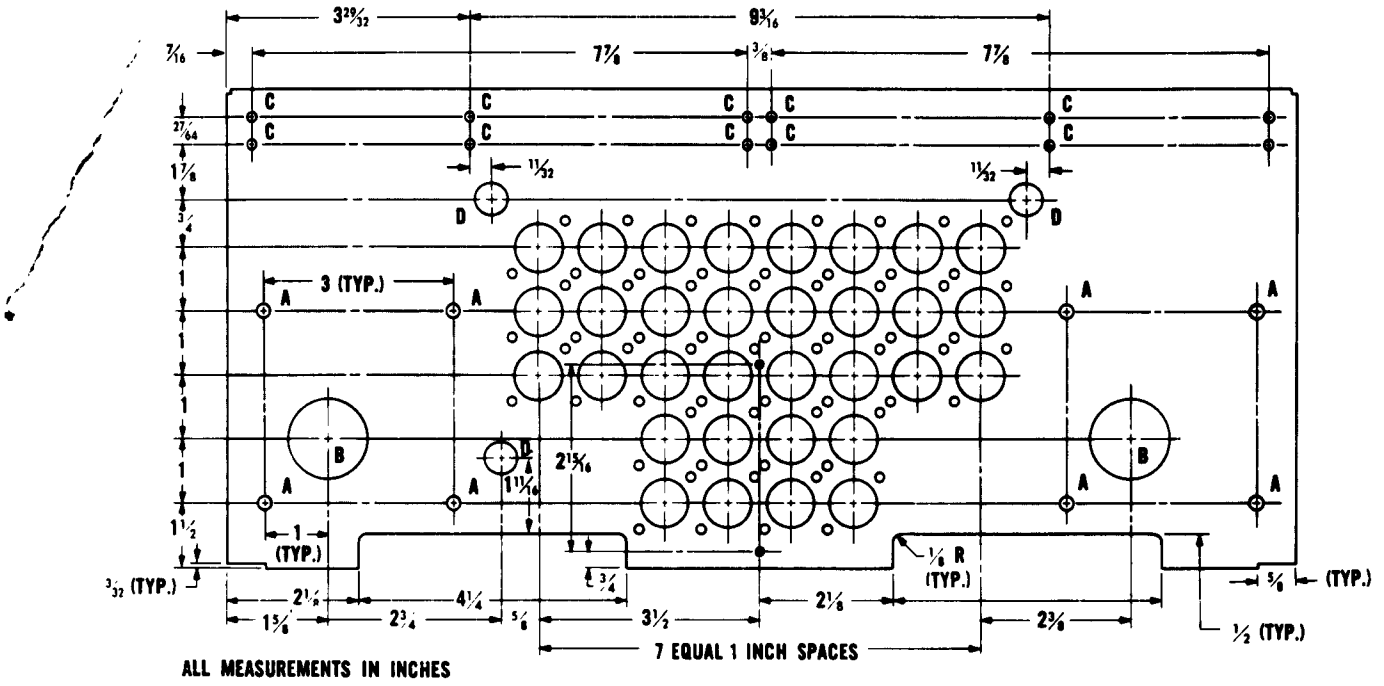
T-964 is identical to T-936 except 13-pin sockets are installed.

Panel layout is shown below



Universal Chassis H-164 contains a chassis with 60-socket holes and a 20-terminal Jones strip. Two front panel heights are available; 3½" (H-164-1) and 5¼" (H-164-2). These front panels have a gray finish and standard Amateur notch.

Layout of Chassis H-164 is shown at top of page

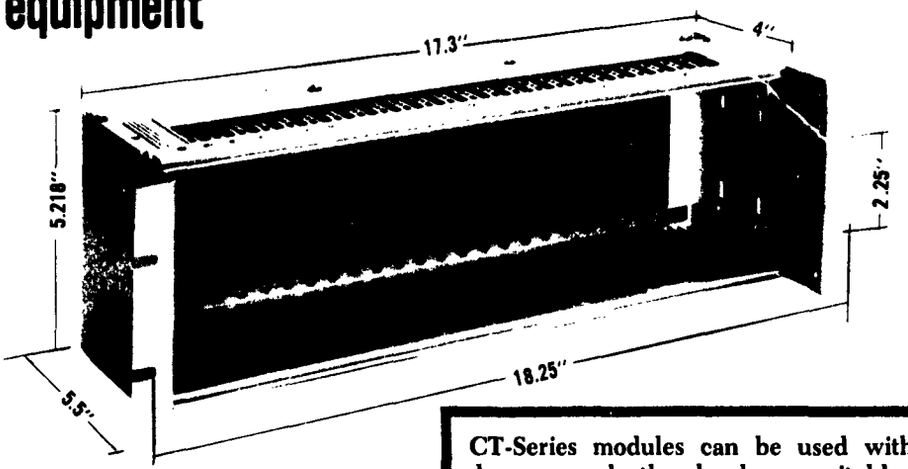


Layout of Chassis H-165

Universal Chassis H-165 contains a chassis with 32 socket holes, a 20-terminal Jones strip, and mounting holes for two ZA-721 power supplies. Two front panel heights are available; 3½" (H-165-1) and 5¼" (H-165-2).

HOLE SCHEDULE		
LETTER	SIZE	QUANTITY
A	7/32	8
B	1¼	2
C	5/32	12
D	½	3

CT related equipment



CARD FILES

H-401 and H-402 (ELCO modified VARIPAK II 9016-2-S)

These sturdy, all-aluminum cases hold up to 27 circuit cards each. They are available from EECo with 82 holes on each mounting panel to permit combinations of equal or variable spacing of the card guides and connectors. We also supply these universal card files with connectors and card guides already mounted as shown in the chart below.

CT-Series modules can be used with card files, card drawers, and other hardware suitable for the 4½"x 5"x 1/16" cards. The hardware shown here is specifically recommended and can be ordered from EECo, using the "H" part numbers shown. For the convenience of companies supplied directly by the manufacturer, the manufacturers' part numbers are shown (in parenthesis).

Card File	Type Connectors	Connectors Installed	Guides Sets Installed
H-401-1	H-404, H-405 or H-406	None	27
H-401-2	Solder-Lug H-404	27	27
H-401-3	Taper-Tab H-405	27	27
H-401-4	Taper-Pin H-406	27	27
H-401-5	H-411, H-412 or H-413	None	27
H-401-6	Solder-Lug H-411	27	27
H-401-7	Wire-Wrap H-412	27	27
H-401-8	Wire-Wrap H-413	27	27
H-401-9	Taper-Pin H-414	27	27
H-402-1	H-404, H-405 or H-406	None	None
H-402-2	H-411, H-412 or H-413	None	None

CONNECTORS

Part #	Connector Type	Connections	For Board Type	Depth Extending From File Mount	Connector Width	Between-Connector Type Tabs	On-Connector Type Tabs
H-404	Single Solder-Lug	22	Ribbon-Type	0.4687"	0.343"	H-408	H-407
H-405	Single Taper-Tab	22	Ribbon-Type	0.4687"	0.343"	H-408	H-407
H-406	Double Taper-Pin	22	Ribbon-Type	0.45"	0.437"	H-408	H-407
H-411	Solder/Taper Tab	35	Varicon	0.73"	0.5312"	H-409	.....
H-412	Wire-Wrap (2 wires)	35	Varicon	1.2"	0.5312"	.....	H-415
H-413	Solder-Lug (3 wires)	35	Varicon	0.87"	0.5312"	.....	H-415
H-414	Taper-Pin	34	Varicon	0.8"	0.5312"	.....	H-415

GUIDE SETS

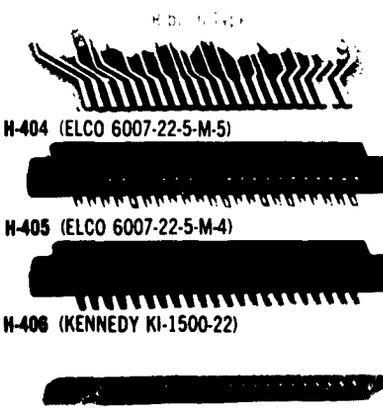
H-403, two guides and snap-in pins per set (ELCO 9016.1201)

Made of polycarbonate with excellent di-electric properties and high mechanical strength. Each guide is held firmly in place by one snap-in pin that permits the guide to be removed and relocated without damage to either guide or plate.

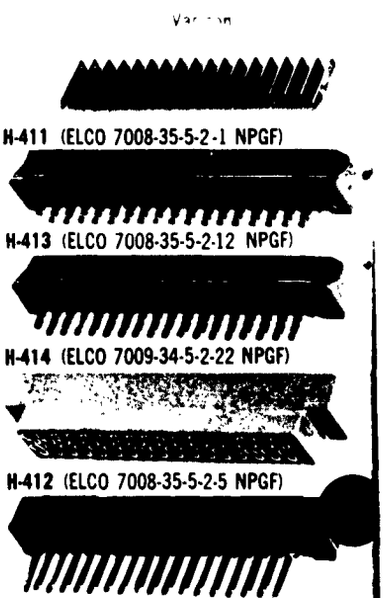
CARD EXTRACTOR

H-410 (PUL-E-ZE Mod. II-1)

These Extractors grip the card edge itself securely enough for a 30-lb. pull. They are made of tough, durable Delrin 100.

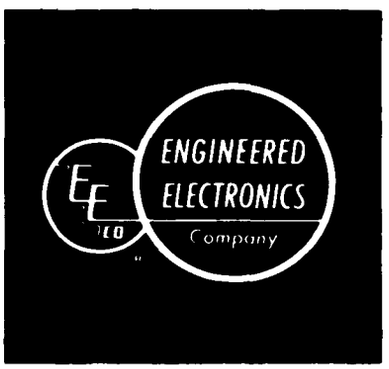


There are seven types of connectors for CT modules available from EECo as shown. Detailed specifications of each type is available in the manufacturer's literature. Separately supplied connectors are furnished with brass screws and nuts.



Special Issue Data Sheets

Special Data sheets cover new information made available before this catalog is republished. When you add material to the back of the book, be sure to list it in the space that is provided in the Index Section.



ENGINEERED ELECTRONICS Company

1441 EAST CHESTNUT AVENUE

SANTA ANA, CALIFORNIA

PHONE: 714-547-5651

TWX: S ANA 5255 • CABLE: ENGELEX

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T-SERIES PRICE LIST

Effective Date: August 1, 1962

ENGINEERED ELECTRONICS Company
1441 EAST CHESTNUT AVENUE
SANTA ANA, CALIFORNIA

NOTE: Terms, FOB point, and footnotes, e.g., ①, ②, etc., will be found at the end of the price lists.

T-SERIES CIRCUIT MODULES

PART NOS.	DESCRIPTION ②①	200-499	100-199	50-99	25-49	10-24	1-9
T-101B	Flip-Flop	14.25	17.30	21.05	27.10	34.80	42.85
T-102A	Flip-Flop	11.55	13.90	16.70	21.45	27.45	33.70
T-103	Flip-Flop	10.75	13.20	16.15	20.85	26.85	33.15
T-104	Multivibrator	12.50	14.35	16.70	21.05	26.50	32.25
T-105A	One-Shot	11.25	13.90	16.90	21.90	28.15	34.75
T-106	Squaring Amplifier	9.55	11.15	13.25	16.80	21.35	26.10
T-107	Crystal Oscillator(10-75Kc)	12.05	13.95	16.50	20.85	26.45	32.25
T-108	Amplifier	16.80	19.15	22.40	28.10	35.45	43.10
T-109	Reset Generator (T-Series)	9.95	11.05	12.70	15.80	17.65	23.85
T-110	Blocking Oscillator	19.10	22.70	27.20	34.75	44.35	54.35
T-111	Emitter Follower	5.50	5.70	6.20	7.45	9.05	10.70
T-112	Emitter Follower, dual	7.75	8.10	9.00	10.90	13.35	15.85
T-113	Emitter Follower, triple	8.65	9.70	11.25	14.05	17.60	21.35
T-114	Emitter Follower	5.70	6.05	6.75	8.25	10.10	12.05
T-115	Emitter Follower, dual	8.10	8.65	9.70	11.80	14.55	17.40
T-116	Emitter Follower, triple	10.80	11.60	13.00	15.85	19.55	23.40
T-117	Pulse Inverter	9.85	12.25	15.15	19.70	25.45	31.50
T-118	Pulse Amplifier	9.35	10.60	12.35	15.50	19.55	23.75
T-120	Relay Driver (0-48V)	16.65	16.90	17.10	19.90	23.65	27.40
T-121	Relay Driver (0-90V)	27.40	27.85	28.50	32.30	37.60	42.80
T-123	Regulator (-7.5V)	15.40	16.15	16.85	17.60	18.30	19.05
T-127	Crystal Oscillator(75-250Kc)	15.45	17.35	20.15	25.10	31.55	38.25
T-128	Relay Driver (0-24V)	16.10	16.80	17.50	18.45	21.70	24.90
T-129	Reset Generator (N-Series)	7.35	9.25	11.45	14.85	19.25	23.85
T-130	Relay Driver (0-30V)	18.35	18.95	19.55	20.25	23.55	26.80
T-134	Driver (0-35V)	16.15	16.45	16.80	19.55	23.25	27.00
T-135	Driver (0-35V)	15.50	16.40	18.25	22.20	27.25	32.45
T-136	Inverter	8.90	9.60	10.80	13.15	16.25	19.45
T-137	Inverter	9.40	9.85	10.85	13.05	15.95	18.95
T-138	Inverter	11.50	12.65	14.45	17.90	22.30	26.85
T-139	Driver (0-30V)	26.60	27.20	27.95	32.70	39.10	45.55
T-140	Crystal Oscillator(1-10Kc)	16.70	18.65	21.50	26.85	33.60	40.65
T-141	Driver (0-45V)	29.35	29.40	31.35	36.90	44.15	51.55
T-157	Flip-Flop	13.30	17.15	21.50	28.35	36.90	45.95
T-161	Emitter Follower, dual	7.35	7.80	8.70	10.55	13.00	15.50
T-162	Flip-Flop	10.95	13.35	16.25	20.95	26.90	33.15
T-163	D C Driver	13.75	15.20	17.45	21.60	26.95	32.50
T-165	Capacity Driver	17.65	20.25	23.75	29.85	37.70	45.85
T-166	One-Shot	10.85	14.20	17.95	23.60	30.80	38.40
T-167	One-Shot	13.95	17.45	21.45	27.90	35.95	44.50
T-170	Relay and Indicator Driver	14.40	14.95	16.35	19.60	23.90	28.25
T-171	Relay and Indicator Driver	16.55	16.85	18.20	21.65	26.15	30.70
T-172	Voltage Comparator	11.30	11.85	13.10	15.80	19.40	23.00
T-173	Bias Supply	14.25	16.05	18.60	23.25	29.20	35.40
T-301A	Gated Flip-Flop	18.95	21.50	25.05	31.40	39.50	47.95
T-302	Capacity Driver	26.65	30.10	34.95	43.70	54.90	66.60
T-303	Flip-Flop	37.25	38.20	41.60	49.70	60.25	71.05
T-304	Emitter Follower	16.70	17.50	19.30	23.30	28.50	33.85
T-305	Video Amplifier	37.30	39.30	43.55	52.70	64.55	76.80
T-306	Squaring Amplifier (5Mc)	33.00	34.15	35.50	41.85	50.25	58.75
T-307	Emitter Follower	23.75	25.45	28.50	34.80	42.95	51.35
T-308	DC Logic	18.15	20.10	23.05	28.55	35.65	42.95
T-309	DC Logic	16.75	18.90	21.95	27.45	34.45	41.80
T-310	DC Logic	14.10	16.05	18.85	23.70	29.95	36.45
T-311	Crystal Oscillator(250Kc-1Mc)	33.95	34.80	36.00	42.25	50.40	58.75

PART NOS.	DESCRIPTION ① ② ③	200-499	100-199	50-99	25-49	10-24	1-9
T-312	Squaring Amplifier (1Mc)	16.60	17.95	20.40	25.10	31.20	37.45
T-314	Multivibrator	20.30	20.90	21.75	25.65	30.70	35.90
T-315	DC Logic	19.20	19.75	21.65	25.95	31.60	37.40
T-317	Crystal Oscillator (10Mc)	20.05	23.90	25.40	31.45	39.30	47.35
T-318	Pulse "And" Gate	31.60	32.65	34.70	41.35	50.00	58.85
T-404	DC Logic	9.85	12.20	15.00	19.45	25.05	30.95
T-405	DC Logic	9.00	10.60	12.60	16.05	20.40	24.95
T-406	DC Logic	10.15	12.45	15.20	19.50	25.10	30.95
T-407	DC Logic	9.45	10.95	12.80	16.20	20.45	24.95
T-410A	Pulse Logic	11.95	13.50	15.70	19.70	24.75	30.05
T-411	Pulse Logic	12.25	15.35	18.90	24.55	31.75	39.30
T-412	Pulse Logic	14.05	18.05	22.55	29.60	38.45	47.75
T-413	Pulse Logic	11.40	13.15	15.45	19.50	24.65	30.05
T-421A	DC Logic	10.75	11.25	12.40	14.85	18.15	21.55
T-422	DC Logic	13.40	15.35	17.95	22.55	28.40	34.55
T-423A	DC Logic	18.00	18.90	20.90	25.30	30.95	36.75
T-424A	Half Adder/Subtractor	13.90	15.75	18.30	22.95	28.80	34.95
T-425A	Diode Logic	5.10	5.55	6.35	7.80	9.70	11.65
T-426A	Diode Logic	5.80	6.30	7.20	8.85	11.00	13.25
T-427A	Diode Logic	5.90	6.65	7.80	9.80	12.30	15.00
T-428A	Diode Logic	6.30	7.30	8.60	10.85	13.70	16.75
T-430	Pulse Logic	10.50	12.50	15.00	19.15	24.45	29.95
T-431	Pulse Logic	11.60	13.95	16.80	21.55	27.55	33.85
T-432	DC Logic	13.35	15.35	18.10	22.90	29.00	35.35
T-433	DC Logic	12.10	14.05	16.60	21.05	26.65	32.50
T-434	DC Logic	11.05	13.45	16.40	21.15	27.20	33.55
T-437	DC Logic	9.40	11.10	13.25	16.90	21.50	26.30
T-438	DC Logic	10.60	12.55	15.05	19.20	24.45	29.95
T-439	DC Logic	10.70	11.10	12.20	14.65	17.90	21.15
T-440	DC Logic	8.90	9.75	11.10	13.65	17.00	20.45
T-441	Full Adder	23.75	28.85	35.15	45.45	58.45	72.05
T-442	Level Restoring "Or" Gate	9.95	13.55	17.55	23.50	30.95	38.80
T-447	Pulse "And" Gate	10.90	12.85	15.35	19.65	25.05	30.70
T-448	Dual Pulse "And" Gate	17.40	20.50	24.50	31.30	39.90	48.90
T-600	Shift Register Logic	11.45	14.95	18.85	24.85	32.40	40.35
T-601	Pulse Logic	19.05	24.70	30.95	40.70	52.95	65.90
T-602	Pulse Logic	18.10	24.15	30.70	40.75	53.30	66.60
T-604	Gated Flip-Flop	14.15	19.30	24.95	33.40	43.95	55.15
T-605	Shift Register Flip-Flop	12.85	16.40	20.40	26.70	34.65	43.00
T-606	Shift Register Flip-Flop	21.05	23.85	27.75	34.75	43.70	53.05
T-607A	Diode Logic	12.60	13.10	14.35	17.25	21.00	24.80
T-608A	Diode Logic	9.95	9.93	11.50	14.45	18.10	21.95
T-609A	Diode Logic	10.45	11.75	13.60	17.00	21.30	25.80
T-610	Shift Register Flip-Flop	14.85	18.45	22.65	29.30	37.80	46.70
T-611	Pulse Gate, triple	10.10	12.35	15.10	19.50	25.15	31.05
T-612	Pulse Logic	15.20	17.50	20.65	26.20	33.20	40.50
T-613	Pulse Logic	15.75	17.90	20.95	26.35	33.30	40.50
T-614	DC Logic	11.40	13.75	16.60	21.25	27.20	33.45
T-620	DC Logic	12.45	14.45	17.00	21.45	27.15	33.10
T-621	DC Logic	11.60	13.80	16.50	21.05	26.85	32.95
T-622	DC Logic	16.30	18.70	21.90	27.60	34.80	42.35
T-623	DC Logic	12.30	14.10	16.50	20.70	26.10	31.70
T-625A	Diode Logic	8.20	9.35	10.95	13.80	17.40	21.20
T-626A	Diode Logic	10.05	11.90	14.35	18.30	23.40	28.75
T-627	Diode Logic	12.25	15.15	18.55	24.05	30.95	37.25
T-628	Diode Logic	15.15	17.20	20.00	25.05	31.50	38.25
T-629	Gated Flip-Flop	14.25	19.75	25.55	34.20	45.10	56.60
T-630	Pulse Logic	17.50	19.20	21.85	27.00	33.50	40.35
T-631A	Diode Logic	10.95	12.35	14.40	18.15	22.85	27.75
T-633	Flip-Flop	16.40	19.20	22.75	28.90	36.70	44.85
T-634	DC Logic	14.35	16.30	18.95	23.75	29.85	36.25
T-635	DC Logic	14.00	16.55	19.75	25.10	31.95	39.10
T-637	Pulse Logic	11.10	13.10	15.65	19.90	25.40	31.05
T-638A	Diode Logic	12.95	15.60	18.90	24.30	31.15	38.35
T-639	Pulse Logic	11.85	13.40	15.65	19.60	24.70	30.05

T-SERIES PRICE LIST

Effective Date: August 1, 1962

ENGINEERED ELECTRONICS Company
1441 EAST CHESTNUT AVENUE
SANTA ANA, CALIFORNIA

PART NOS.	DESCRIPTION (1) (2) (3)	200-499	100-199	50-99	25-49	10-24	1-9
T-640	Pulse Logic	11.95	13.45	15.70	19.65	24.75	30.05
T-641	DC Logic	16.60	16.95	17.45	20.35	24.25	28.20
T-642	DC Logic	13.00	13.95	15.60	19.15	23.60	28.20
T-643	Flip-Flop	23.60	26.60	30.90	38.60	48.45	58.70
T-644	Flip-Flop	19.75	23.00	27.30	34.55	43.85	53.55
T-645	NOR Circuit	11.15	12.95	15.35	19.50	24.75	30.30
T-646	RS Flip-Flop	11.25	15.40	19.90	26.60	35.00	43.85
T-647	Flip-Flop	19.45	22.15	25.80	32.40	40.75	49.55
T-648	Flip-Flop	18.10	21.10	25.00	31.65	40.10	49.00
T-650	DCTL "And" Gate	17.55	18.55	20.55	24.80	30.45	36.20
T-651	DCTL "Or" Gate	12.90	14.50	16.65	20.75	26.00	31.45
T-652	Emitter Follower	10.60	12.50	14.95	19.15	24.40	29.90
T-653	DCTL "And/Or" Gate	12.30	13.40	15.25	18.85	23.45	28.20
T-801A	Flip-Flop	24.85	26.75	30.10	36.80	45.50	54.45
T-802	DC Logic	27.20	28.80	32.20	39.20	48.30	57.70
T-803	DC Logic	22.05	23.40	26.10	31.65	38.95	46.45
T-805	DC Logic	32.45	34.75	38.90	47.55	58.60	70.10

CRYSTAL AND COMPONENT OVENS

PART NOS.	DESCRIPTION (1) (2)	PRICE
H-143-1	Oven only, 115V heater voltage, will hold 2 crystals for use with T-107 and/or T-127 in frequency range 10Kc to 250 Kc.	23.50
H-143-2	Same as H-143-1 except 28V heater voltage.	23.50
H-143-3	Same as H-143-1 except 12V heater voltage.	23.50
H-143-4	Same as H-143-1 except 6V heater voltage.	23.50
H-145-31	10Kc crystal for use with T-107.	68.50
H-146-2	100Kc crystal for use with T-127.	25.00
H-149-1	Oven only, 115V heater voltage, will hold a T-107 and matching crystal for frequency range 10Kc to 45Kc or with a T-311 and matching crystal for frequency range 250Kc to 899.99Kc.	114.00
H-149-2	Same as H-149-1 except 28V heater voltage.	114.00
H-150-1	Oven only, 115V heater voltage, will hold either a T-107 or a T-127 and matching crystal for frequency range 45Kc to 250Kc or with a T-311 and matching crystal for frequency range 900Kc to 1Mc.	114.00
H-150-2	Same as H-150-1 except 28V heater voltage.	114.00
H-160-10	1Mc crystal for use with T-311.	19.30
H-167-8	1Kc crystal for use with T-140.	121.50

T-SERIES SOCKETS, CONTAINERS, ETC.

PART NOS.	DESCRIPTION (2) (1)	10-24	1-9
T-906	T-Series Container, 13-pin, w/2 discs	2.55	2.60
T-908	T-Series Container, 13-pin, w/3 discs	2.95	3.00
T-909	T-Series 13-pin socket (Cinch #54A14775 with keying plug in pin #10) for 1/8" panel.	.45 (5)	(5)
T-910	T-Series 9-pin socket (EBY #9713-32) for 18-gauge chassis.	(6)	.25 (6)
T-913	T-Series Standard Pattern Disc (use w/T-904, T-906, T-908, if extra discs are needed).	(5)	.60 (5)
T-937	T-Series 13-pin socket, T-909, with T-959 spacer for 18-gauge chassis.	(5)	.60
T-959	Spacer. Adapts T-909 socket for use with 18-gauge chassis. (3)	.15	.15

CT-SERIES CIRCUIT BOARD MODULES

Terms, FOB point, and footnotes, e.g., (1) , (2) , etc., will be found at the end of the catalog price lists.

The prices listed below are for units with standard tin-plated connectors. Add $2.00 per unit when Varicon, Gold-plated, or Rhodium-plated special connectors are required.

PART NOS.	DESCRIPTION (1) (2)	200-499	100-199	50-99	25-49	10-24	1-9
CT-101B-3	Three RST Flip-Flops	34.75	36.20	39.00	40.40	48.80	77.15
CT-102A-4	Four T Flip-Flops	34.10	34.40	37.65	39.40	40.65	80.90
CT-104-2	Two Multivibrators	20.85	21.30	22.20	23.30	25.30	50.45
CT-106-4	Four Squaring Amplifiers	29.95	31.45	32.65	33.20	37.90	62.65
CT-109-4	Four Reset Generators	34.00	35.90	37.80	40.20	42.90	57.25
CT-111-9	Nine PNP Emitter Followers	19.70	19.90	20.40	20.90	25.30	38.45
CT-114-9	Nine NPN Emitter Followers	29.20	30.80	31.60	32.10	33.50	42.10
CT-134-4	Four Relay and Indicator Drivers.	55.20	58.40	61.40	62.60	63.80	77.40
CT-136-4	Four Inverters	20.75	21.15	22.65	23.60	26.00	49.95
CT-162-4	Four RS Flip-Flops	37.45	39.50	41.60	44.80	50.95	79.55
CT-163-3	Three DC Drivers	37.20	39.20	43.30	49.75	56.35	58.50
CT-165-4	Four Capacity Drivers	67.25	68.10	68.70	76.95	90.25	110.05
CT-166-4	Four One-Shot Multivibrators	40.50	41.00	41.35	53.95	62.60	92.15
CT-302-2	Two Capacity Drivers	67.20	70.80	72.60	79.00	94.40	102.45
CT-304-4	Four Complementary Emitter Followers.	57.20	60.20	63.40	66.40	73.40	86.65
CT-306-2	Two Squaring Amplifiers	59.60	62.70	64.90	67.40	79.50	90.00
CT-307-4	Four Dual Complementary Emitter Followers.	81.40	85.60	90.20	96.80	108.40	129.90
CT-421A-4	Four "Exclusive-Or" Gates	29.40	29.95	31.05	32.00	34.85	51.80
CT-430-4	Four Pulse Mixer Amplifiers	36.00	38.00	40.00	41.50	43.90	71.80
CT-448-2	Two Dual Pulse "And" Gates	31.45	33.05	38.95	46.55	49.70	58.70
CT-605-3	Three Shift Register Flip-Flops.	29.80	31.80	32.85	36.70	48.05	77.40
CT-606-2	Two Shift Register Flip-Flops.	28.70	30.25	31.20	33.30	41.70	63.65
CT-641-2	Two Dual DCTL "And" Gates	29.90	31.50	32.20	33.20	38.70	46.70
CT-642-2	Two Dual DCTL "Or" Gates	22.85	23.40	24.50	25.30	26.75	33.80
CT-645-2	Two DCTL "Nor" Gates	20.10	21.20	24.60	29.20	30.80	35.70
CT-650-2	Two Dual DCTL "And" Gates	31.65	33.35	35.25	39.05	47.10	50.20
CT-651-2	Two Dual DCTL "Or" Gates	23.30	24.50	27.55	30.65	31.10	37.75
CT-801-2	Two Flip-Flops	40.40	41.35	42.90	43.60	46.25	54.60
CT-802-2	Two Dual DCTL "And" Gates	49.10	51.70	54.70	61.20	74.50	88.80
CT-805-2	Two Dual "Exclusive-Or" Gates.	49.60	60.35	61.55	62.40	63.70	70.30

T-SERIES PRICE LIST

Effective Date: August 1, 1962

ENGINEERED ELECTRONICS Company
1441 EAST CHESTNUT AVENUE
SANTA ANA, CALIFORNIA

SYSTEM BREADBOARD EQUIPMENT AND ACCESSORIES

Complete rack-mounted or suitcase-mounted System Breadboard Equipment can be purchased in kit form as H-180 or H-181 with a dash number appended to define the specific kit; these dash numbers are assigned at the factory when a specific quotation is made. Each kit consists of specified plug-in circuit modules and one or more of each of the following items

PART NOS.	DESCRIPTION	PRICE
Z-97221	Portable Digital System Breadboard, includes 1 H-153, 1 T-965A, 2 T-958, 4 T-927, 2 T-918, 1 Z-97432, and cabling.	2373.00
Z-97432-2	Power Supply for Z-97221 (not sold separately)	488.00
Z-97597A	Rack-Mounted Digital System Breadboard, includes 1 H-155, 1 T-965A excluding plug-ins, 2 T-958, 1 T-918, 3 T-927, 1 ZA-720.	2175.00
Z-97598	Rack-Mounted Digital System Breadboard, includes 1 H-155, 2 T-958, 2 T-918, 4 T-927.	1402.00
Z-97599A	Rack-Mounted Digital System Breadboard, includes 1 H-155, 1 T-965A excluding plug-ins, 2 T-958, 1 T-918, 3 T-927, 1 Z-97617A-2.	1799.00
Z-97617A-2	Rack-Mounted Power Supply (+12V, -12V, -3V, -11V)	499.00
Z-101663	Power Panel for H-189 (not sold separately)	428.00
T-915	Indicator Panel, 1 3/4" X 19", w/16 R-1010 Minisig Indicators (Neon) and banana jacks for input signals. Indicators light when input signal is -3V. Gray finish, Amateur notch. (7)	234.00
T-916	Indicator and Tie Point Panel, 1 3/4" X 19", W/8 R-1010 Minisig Indicators (Neon), plus 8 dual binding posts for external parts such as resistors, diodes, capacitors, etc. T-916 is similar to T-915. Indicators light when input signal is -3V. Binding posts will accept T-920 and also standard banana plug patch cords. Gray, Amateur notch. (7)	174.00
T-917	Indicator Panel. Same as T-915 except uses R-341 Minisig Indicators (Filament). (7)	261.00
T-918	Indicator and Tie Point Panel. Same as T-916 except uses R-341 Minisig Indicators (Filament). (7)	188.00
T-919/xxx	Circuit Symbol Card. Plastic encased. Holes are punched in card to match field of banana jacks on T-927 panel. Order by T-Series circuit number in place of xxx. For example: T-919/101B is card for T-101B Flip-Flop. (7)	.50
T-920	Power Plug. Black, dual banana plug with shorting bar between pins. Used w/T-927 panels and T-919/xxx circuit symbol cards. (7)	1.35
T-927	System Development Panel, 5 1/4" X 19" w/8 nine-pin sockets and 8 thirteen-pin sockets. Used with T-919/xxx circuit symbol cards and T-920 power plugs for breadboarding T-Series systems; using either 9-pin or 13-pin units. Panel will accept up to 8 circuits at one time.	95.00
T-928	Component Plug. Red. Similar to T-920 power plug but w/o shorting bar. Used with T-916 and T-918. Holds resistor, capacitor, or diode, and plugs into dual binding post. (7)	1.70
T-929	Component Plug. Yellow. Same as T-928 except color. (7)	1.70
T-930	Component Plug. Blue. Same as T-928 except color. (7)	1.70

PART NOS.	DESCRIPTION ① ②	PRICE
T-946	Circuit Storage Box.	10.00
T-947	Accessory Storage Box.	7.50
T-958	Indicator and Tie Point Panel, same as T-916 except uses R-342 indicators. ⑦	203.00
T-965A	Signal Generator Panel, w/o plug-ins	195.00
	w/ plug-ins	301.00
H-101	Black Patch Cord, 4" long	1.30
H-106	Black Patch Cord, 8" long	1.30
H-107	Red Patch Cord, 8" long	1.30
H-108	Blue Patch Cord, 8" long	1.30
H-109	Green Patch Cord, 8" long	1.30
H-110	Yellow Patch Cord, 8" long	1.30
H-111	Black Patch Cord, 12" long	1.30
H-112	Red Patch Cord, 12" long	1.30
H-113	Blue Patch Cord, 12" long	1.30
H-114	Green Patch Cord, 12" long	1.30
H-115	Yellow Patch Cord, 12" long	1.30
H-116	Black Patch Cord, 18" long	1.30
H-117	Red Patch Cord, 18" long	1.30
H-118	Blue Patch Cord, 18" long	1.30
H-119	Green Patch Cord, 18" long	1.30
H-120	Yellow Patch Cord, 18" long	1.30
H-153	Suitcase (with cabling) for Z-97221	225.00
H-154	Rack for Rack-Mounted System Breadboards, 19" panels, 28" vertical panel space, 32" overall height, gray-wrinkle finish.	20.00
H-155	Same as H-154 except includes power cabling (sold only as part of System Breadboard Kit).	125.00
H-159	Right-angle Bracket to accommodate 13-pin decade in T-927. ⑦	10.00
H-179	Adapter to accommodate non-standard-power-connection special circuits to T-927. ⑦	5.00
H-188	Suitcase with cabling for H-189.	147.00
H-189	Portable Digital Breadboard System, includes 1 H-188, 1 T-965A, 3 T-927, 2 T-958, 1 Z-101663, and cabling.	1422.00

POWER SUPPLIES

PART NOS.	DESCRIPTION ① ②	PRICE
ZA-720	Power Supply, dual, 12VDC, 5 amp	880.00
ZA-721	Power Supply, 12VDC, 1 amp	160.00
ZA-723	Power Supply, 12VDC, 300 ma	150.00
ZA-724	Power Supply, 12VDC, 3 amp	300.00
ZA-725	Power Supply, 12VDC, 1 amp	160.00
ZA-727	Power Supply, +12VDC, 100 ma	110.00
ZA-728	Power Supply, 12VDC, 5 amp	400.00
ZA-729	Same as ZA-728 except bolted to 5 1/4" panel. Half of chassis is supplied w/o sockets to accommodate smaller power supplies or plug-in units.	450.00

T-SERIES PRICE LIST

Effective Date: August 1, 1962

ENGINEERED ELECTRONICS Company
1441 EAST CHESTNUT AVENUE
SANTA ANA, CALIFORNIA

PANELS AND CHASSIS

* Prices for larger quantities on request.

PART NOS.	DESCRIPTION (1) (2)	10-24	1-9
T-901	Panel 51 socket holes, w/o sockets, 3 1/2" X 19". Gray finish Amateur notch.	*	22.10
T-902	Panel, 51 socket holes, w/9-pin sockets, 3 1/2" X 19". Gray finish, Amateur notch. (4)	40.95	43.20
T-903	Panel, 51 socket holes, w/9-pin sockets and buss wired for power, 3 1/2" X 19". Gray finish, Amateur notch. (4)	58.20	60.40
T-932-1	Panel, 38 socket holes, w/o sockets. Holes are spaced to accept IERC Base T6-1001 for IERC Shield T6-1025-3. Panel is 3 1/2" X 19". Gray finish, Amateur notch.	*	21.90
T-932-2	Same as panel T-932-1 except 38 IERC Shield T6-1025-3, 38 IERC Base T6-1001, and 38 sockets are furnished, unmounted:		
	with 9-pin sockets	*	183.00
	with 13-pin sockets	*	195.00
T-932-3	Same as panel 932-2, except that the sockets furnished are combination sockets.	*	207.00
T-933-1	Panel, 45 socket holes, w/o sockets. Holes are spaced to accept Cinch-Jones Base # 9SB1 or EBY Base # 9716-11 for Elco Shield # 195V. Panel is 3 1/2" X 19". Gray finish, Amateur notch.	*	21.90
T-933-2	Same as panel # T-9331-1 except 45 each of the following are furnished unassembled: 9 or 13 pin sockets as specified, Cinch-Jones Base # 9SB1 or EBY Base # 9716-11 as specified, and Elco Shield # 195V:		
	with 9-pin sockets	*	63.00
	with 13-pin sockets	*	77.00
	with combination sockets	*	91.00
T-934	Panel, 70 socket holes on 1" centers, w/o sockets. Panel is 5 1/4" X 19". Gray finish, Amateur notch.	25.00	26.80
T-935	Panel, 70 socket holes, w/9-pin sockets. Otherwise same as T-934. (4)	52.20	54.80
T-936	Panel, 70 socket holes, w/9-pin sockets and buss wired for power. Otherwise same as T-934. (4)	88.65	91.50
T-961	Panel, 51 socket holes, w/13-pin sockets, 3 1/2" X 19". Gray finish, Amateur notch. (4)	56.60	58.85
T-962	Panel, same as T-961 except sockets are buss wired for power and ground. (4)	73.85	75.90
T-963	Panel, 70 socket holes, w/13-pin sockets, 3 1/2" X 19" Gray finish, Amateur notch. (4)	69.20	71.80
T-964	Panel, same as T-963 except sockets are buss wired for power and ground. (4)	105.65	108.50
H-164-1	Universal Chassis w/60 socket holes, 20-terminal Jones strip, and 3 1/2" front panel.	*	65.00
H-164-2	Same as H-164-1 except 5 1/4" front panel.	*	70.00
H-165-1	Universal Chassis w/32 socket holes, 20-terminal Jones strip, mounting holes for 2 ZA-721 Power Supplies, and 3 1/2" panel.	*	65.00
H-165-2	Same as H-165-1 except 5 1/4" panel. Includes switch for power and 2 indicating-type fuseholders.	*	70.00

PRINTED CIRCUIT CARD HARDWARE

PART NOS.	DESCRIPTION (2) (1)	PRICE
H-401-1	Card File for all connectors except Varicon types. Guides installed for 27 connectors; drilled rails supplied for connector mounting. (Modified Elco Varipak II, part number 9016-2-S) connectors not supplied.	32.60
H-401-2	Same as H-401-1 with 27 solder lug connectors, type H-404, installed.	141.95
H-401-3	Same as H-401-1 with 27 taper tab connectors, type H-405, installed.	141.95
H-401-4	Same as H-401-1 with 27 taper pin connectors, type H-406, installed.	109.55
H-401-5	Same as H-401-1 except for use with Varicon connector only.	32.60
H-401-6	Same as H-401-1 with 27 solder lug/taper tab connectors, type H-411, installed.	220.25
H-401-7	Same as H-401-1 with 27 wire-wrap (two wires) connectors, type H-412, installed.	220.25
H-401-8	Same as H-401-1 with 27 wire-wrap (three wires) connectors, type H-413, installed.	220.25
H-401-9	Same as H-401-1 with 27 taper pin connectors, type H-414, installed.	267.50
H-402-1	Card File for all connectors except Varicon types. Guides and connectors not installed. Rails supplied drilled for all combinations of guide spacings. (Modified Elco Varipak II, part number 9016-2-S).	24.50
H-402-2	Same as H-402-1 except for use with Varicon connectors only.	24.50
H-403	Guide sets for card file - 2 guides per set. (Elco part number 9016.1201)	.30 per set
H-404	Solder lug connector, 22 contacts. (Elco part number 6007-22-5-M-5)	4.05
H-405	Taper tab connector, 22 contacts. (Elco part number 6007-22-5-M-4)	4.05
H-406	Taper pin connector, 22 contacts. (Kennedy part number KI-1500-22)	2.85
H-407	Polarizing key, between contact type for H-404 and H-405 connectors. (Elco part number 6002.3124)	.05
H-408	Polarizing key, on contact type for H-404 and H-405 connectors. (Elco part number 6007.3419)	.05
H-409	Polarizing key, on contact type for H-406 connector.	.10
H-410	Card extractor (Products for Industry PUL-E-ZE Mod. II-1)	13.00
H-411	Solder/taper tab connector, Varicon type, 35 contacts. (Elco part number 7008-35-5-2-1 NPGF)	3.90
H-412	Wire-wrap connector (two wires), Varicon type, 35 contacts. (Elco part number 7008-35-5-2-5 NPGF)	3.90
H-413	Wire-wrap connector (three wires), Varicon type, 35 contacts. (Elco part number 7008-35-5-2-12 NPGF)	3.90
H-414	Taper pin connector, Varicon type, 34 contacts. (Elco part number 7009-34-5-2-22 NPGF)	6.25
H-415	Polarizing key, between contact type for H-411, H-412, H-413, and H-414 connectors. (Elco part number 5006.3414)	.05

ORDERING INFORMATION

FOOTNOTES

① Prices in Western Europe are 5% higher plus C.I.F. Port of Entry.

② Description information listed does not necessarily correspond to the **actual marking** on parts because of limited space on the part. When ordering, use the **part number** and a brief parts description. For example, order as "ZA-720 Power Supply," "T-166 One Shot" etc.

③ All T-600 and T-800 Series modules are furnished with the mating 13-pin connector (T-937) **free of charge.** See listings for T-937 and T-909 if additional sockets and/or different mounting style sockets are required.

④ May be supplied with other combinations of sockets on special order, must be quoted by factory.

⑤ Minimum order quantity 10.

⑥ Minimum order quantity 20.

⑦ Used with System Development Panels T-927.

TERMS AND CONDITIONS

Terms are net 30 days. Prices are FOB Santa Ana, California. Prices and specifications are subject to change without notice. EECo assumes no obligation to incorporate production changes into previously delivered equipment.

WARRANTY

Engineered Electronics Company hereby warrants standard catalog items of our manufacture to be free from defects. If **at any time** a module fails in normal service due to defective parts, workmanship or packaging, Engineered Electronics Company will repair or replace the module without charge providing required parts are still available. In addition, modules damaged by misuse, accident, neglect, or improper installation, will be repaired at cost.

GOVERNMENT SOURCE INSPECTION

The following additional charges apply for Government Source Inspection of **finished** items (not components).

a. Charge for catalog units: $5.00 set up for each circuit plus $ .50 per item; not to exceed $25.00 for any circuit.

b. Charge for power supplies: $15.00 set up plus $5.00 per unit regardless of quantity.

EECo SALES REPRESENTATIVES

MAINE, NEW HAMPSHIRE RHODE ISLAND, VERMONT, MASSACHUSETTS

White Sales Company
1211 Highland Avenue
Needham 92, Massachusetts
Telephone: 444-3676
Area Code: 617

CONNECTICUT, WESTERN MASSACHUSETTS

White Sales Company
P. O. Box 122
Berlin, Connecticut
Telephone: 224-0423
Area Code: 203

WESTERN AREA UPPER NEW YORK STATE

R. P. Kennedy Company, Inc.
15 Warrington Drive
Rochester 18, New York
Telephone: 271-6322
Area Code: 766

EASTERN AREA UPPER NEW YORK STATE

R. P. Kennedy Company, Inc.
P. O. Box 54
Fayetteville, New York
Telephone: 637-9531
Area Code: 716

R. P. Kennedy Company, Inc.
92 Academy Street
Poughkeepsie, New York
Telephone: 471-4430
Area Code: 914

NEW YORK CITY AND SURROUNDING BOROUGHS, NORTHERN NEW JERSEY

Kenneth E. Hughes Company
4808 Bergenline Avenue
Union City, New Jersey
Telephone: 867-3204
Area Code: 201

SOUTHERN NEW JERSEY, EASTERN PENNSYLVANIA

Kenneth E. Hughes Company
134 Kings Highway East
Haddonfield, New Jersey
Telephone: 428-2727
Area Code: 609

FLORIDA, GEORGIA

Col-Ins-Co-Incorporated
5728 Precision Drive
Orlando, Florida
Telephone: 241-1501
Area Code: 305

NORTH CAROLINA, SOUTH CAROLINA, EASTERN TENNESSEE

Col-Ins-Co-Incorporated
3925 Guinevere Lane
Winston-Salem, North Carolina
Telephone: 722-7112
Area Code: 919

ALABAMA, MISSISSIPPI, WESTERN TENNESSEE

Col-Ins-Co-Incorporated
15-16 Hutchins Bldg.
Huntsville, Alabama
Telephone: 539-1771
Area Code: 205

OHIO, MICHIGAN, WESTERN PENNSYLVANIA

M. P. Odell Company
26614 Center Ridge Road
Westlake, Ohio
Telephone: 871-8000
Area Code: 216

DAYTON AREA

M. P. Odell Company
2676 Salem Avenue
Dayton 6, Ohio
Telephone: 277-4441
Area Code: 216

WESTERN PENNSYLVANIA

M. P. Odell Company
P. O. Box 10595
Pittsburgh 35, Pa.
Telephone: 371-1231
Area Code: 412

MICHIGAN

M. P. Odell Company
10531 West McNichols Road
Detroit 21, Michigan
Telephone: 862-1573
Area Code: 313

ILLINOIS, INDIANA, WISCONSIN, MISSOURI, NORTHERN KENTUCKY

R. Edward Stemm Incorporated
5681 West Lake Street
Chicago 44, Illinois
Telephone: 379-2700
Area Code: 312

MINNESOTA, IOWA

R. Edward Stemm Incorporated
2713 Lyndale Avenue South
Minneapolis 8, Minnesota
Telephone: 822-8404
Area Code: 612

TEXAS, OKLAHOMA, KANSAS, ARKANSAS, LOUISIANA

Robert R. Thomas Company
Suite 106
1066 West Mockingbird Lane
Dallas 7, Texas
Telephone: 631-5666
Area Code: 214

ARIZONA

Western Engineering Company
1644 West Hatcher Road
P. O. Box 9337
Phoenix 20, Arizona
Telephone: 944-0431
Area Code: 602

NEW MEXICO

Western Engineering Company
119 Richmond Drive SE
Albuquerque, New Mexico
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COLORADO, UTAH, SOUTHERN IDAHO

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Willer Engineering & Sales Company
1800 Avenue Road
Toronto 12, Ontario, Canada
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